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A dedicated processor for the self-test of BST boards

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Boundary Scan Test (BST) appeared as an answer to the problem of testing complex printed circuit boards (PCBs), where high complexity components and advanced packaging technologies, seriously restrict the usefulness of conventional testing methods. It requires every functional pin of each IC to have an associated BS cell, allowing complete controllability and observability of the corresponding electrical node. All these cells are interconnected as a chain scanning the complete PCB, and implementing the equivalent of an electronic bed-of-nails.

The complete BST infrastructure allows the implementation of straightforward procedures for testing board interconnects, and for triggering on-chip self-test mechanisms. The availability of this infrastructure allows the implementation of board self-test features, but requires the development of a dedicated controller, with access to board structural information, and to a description of the test patterns to be applied.

The presentation will describe the architecture of a minimum instruction set BST processor. The choice of a minimum set of resources allows a large ROM to be included in the same package, which may be necessary for higher complexity boards. The requirements for the automatic generation of the personality file defining the contents of this ROM will also be discussed, which will in turn make it possible to automatically generate a dedicated self-test processor for a given board design.

A first version of this processor was fabricated in 1.5μm CMOS technology, requiring an area of approximately 11 sq. mm. This circuit was designed as part of a PhD Dissertation, and was manufactured for the University of Porto under the EUROCHIP programme.

Setembro / Outubro 91

A Dedicated Processor for the Self-Test of BST Boards

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This work describes the architecture of a dedicated processor for the self test of BST boards. Prototype versions of this processor have been manufactured for the University of Porto under the EUROCHIP program.

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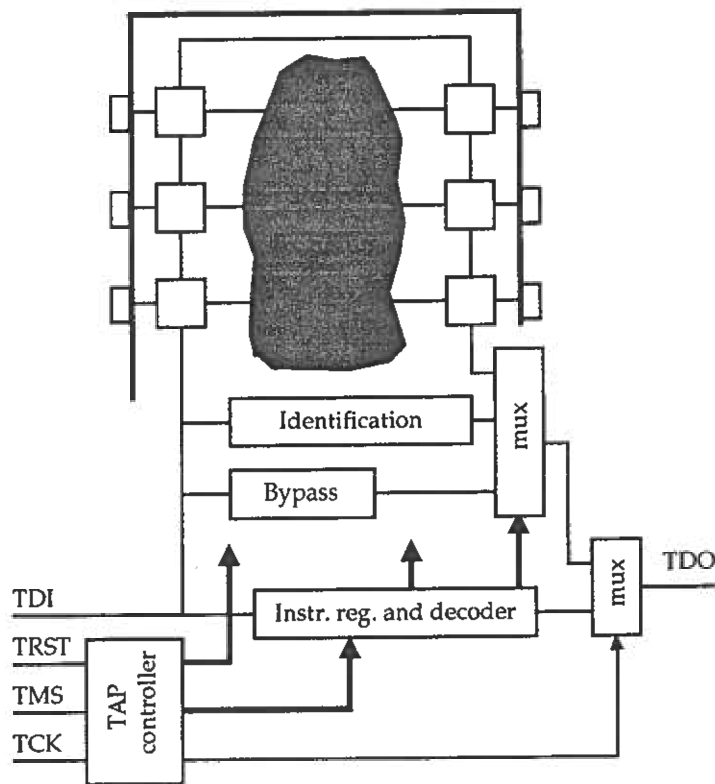

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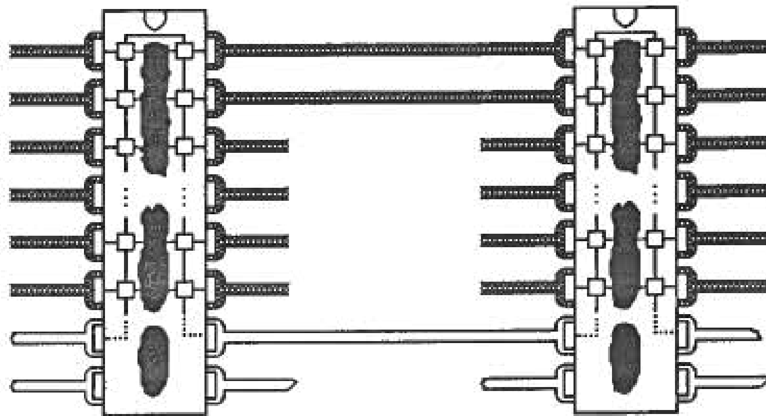

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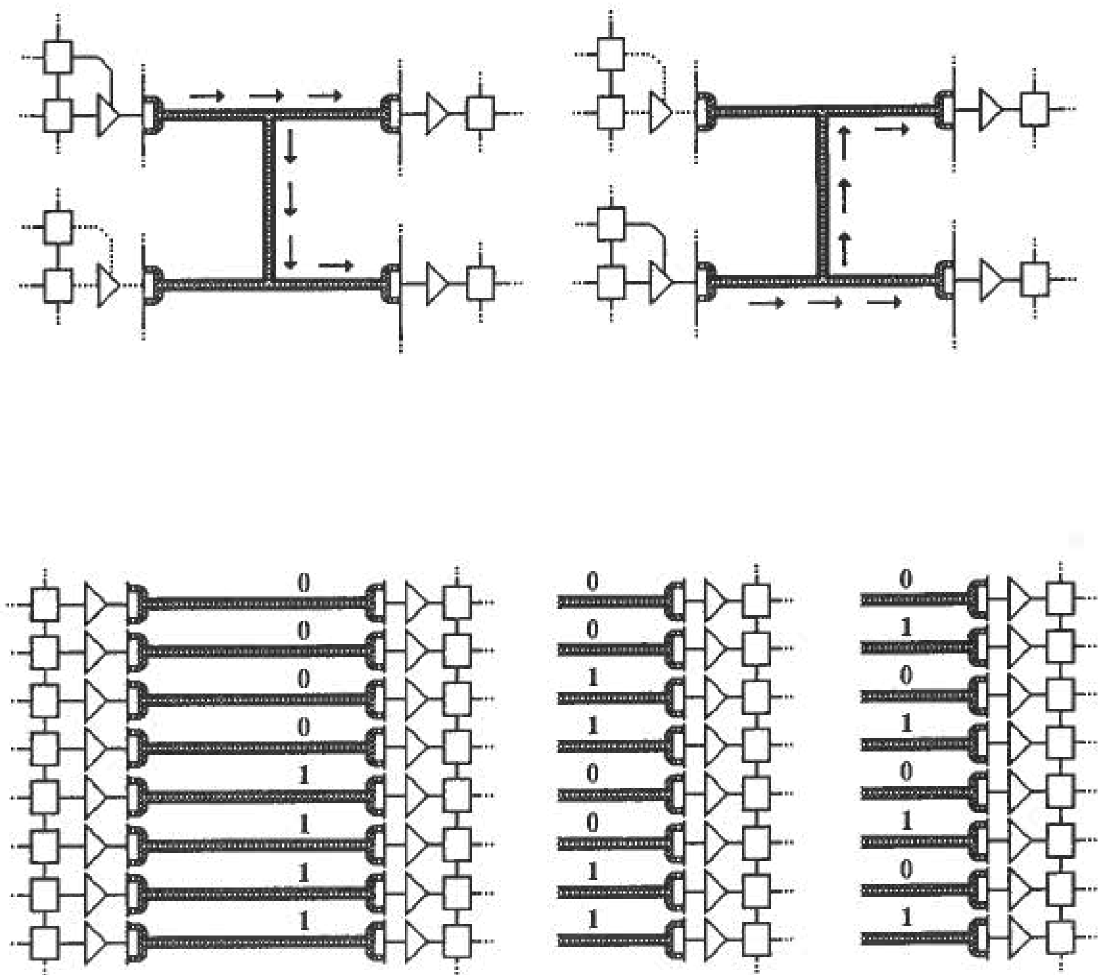
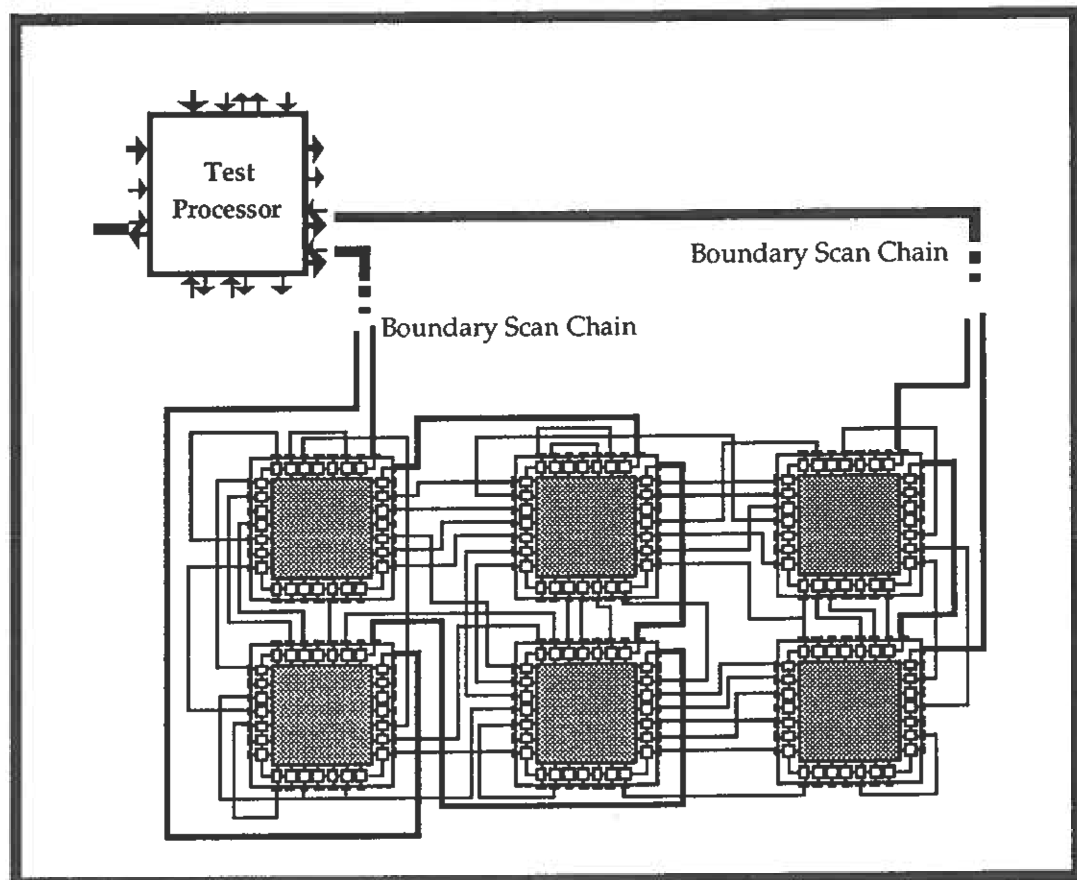


The availability of this infrastructure allows the implementation of board self-test features, but requires the existence of a dedicated controller (test processor).



The instruction set of this processor allows the implementation of all elementary actions required to control the BST infrastructure, such as initializing the BST logic, shifting bit strings through the BST chain, etc.

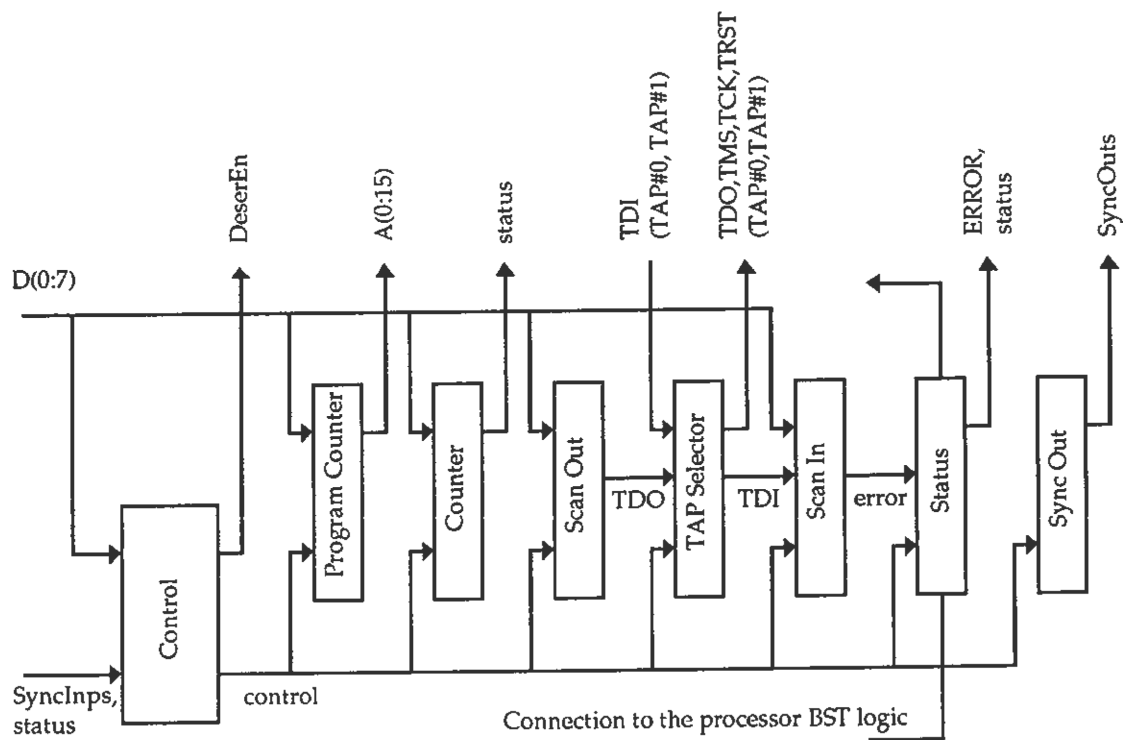
Control of the BST infrastructure	
Procedure	**Instruction**
Applies N test clock cycles (N is the value loaded in an internal counter).	**NTCK**
N bits will be shifted into the BST chain (N is loaded in an internal counter). Bits shifted out of the BST chain are not compared.	**NSHF**
N bits will be shifted into the BST chain (N is the value loaded in an internal counter). Bits shifted out of the BST chain are compared with their expected value. A mask is used to discard don´t care bits.	**NSHFCP**
Forces an asynchronous reset through the active /TRST output.	**TRST**
Forces a state transition in the internal BST logic of each component.	**TMS0, TMS1**
Selects which TAP will be controlled by following instructions.	**SELTAP0, SELTAP1**

These instructions should be complemented with a number of other instructions, addressing the control of internal processor resources, and allowing the synchronization with external test equipment.

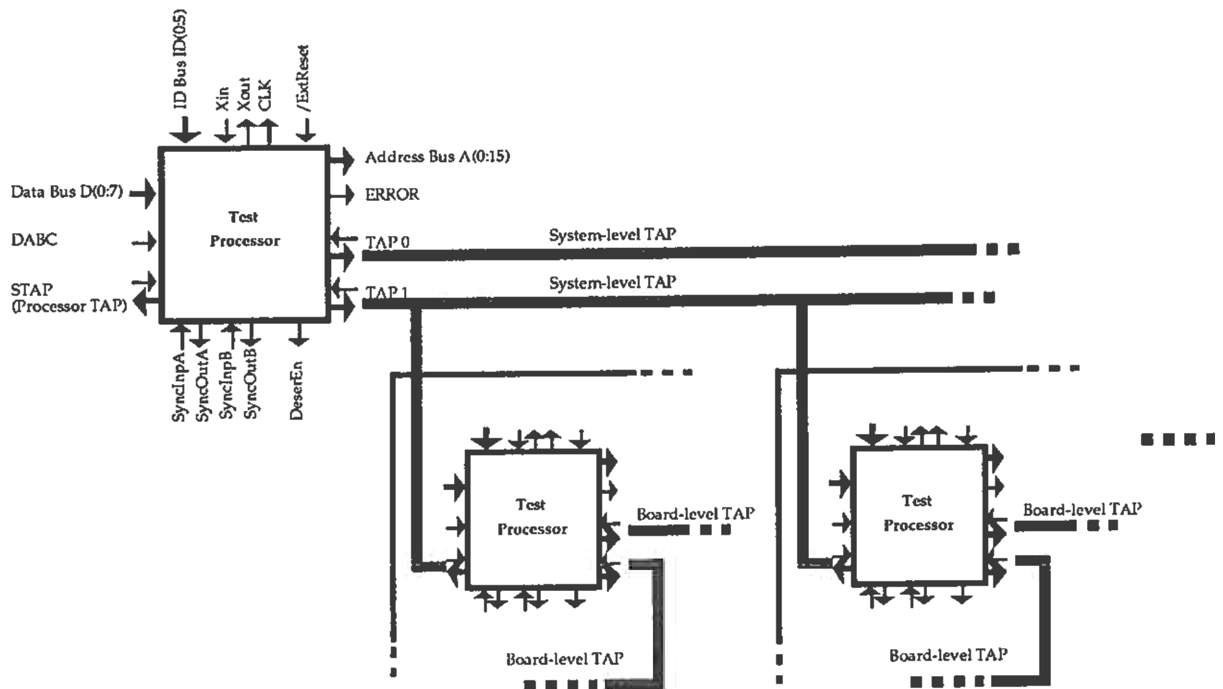
Control of internal processor resources	
Procedure	**Instruction**
Loads an internal counter with the number of test clock cycles to be applied.	**LD CNT, data**
Allows selection of the active error flag.	**SERFLG0, ... , SERFLG7**
Leaves the normal test sequence, if an error is found.	**JPE address**
Leaves the normal test sequence, if an error is not found.	**JPNE address**
Unconditional stop of test program execution.	**HALT**

Test execution synchronization	
Procedure	**Instruction**
Forces a logical value (0,1) on the specified synchronism output (A,B).	**SSA0, SSA1, SSB0, SSB1**
Waits for a logical value (0,1) on the specified synchronism input (A,B).	**WSA0, WSA1, WSB0, WSB1**

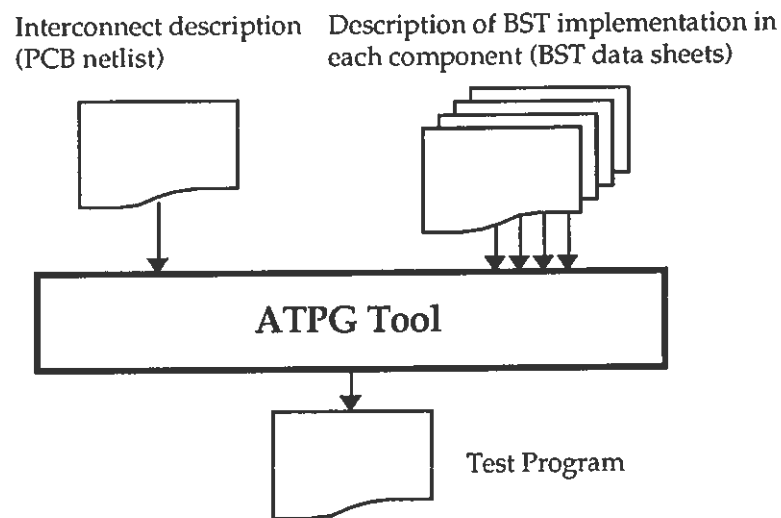
This instruction set determines the existence of a set of blocks which constitute the architecture of a test processor optimized for the control of the BST infrastructure.



The test processor is itself a BST component, which allows several processors to be used in a hierarchical configuration.



Access to a set of files describing structural information (board netlist) and a description of the BST implementation in each component, allows the automatic generation of the test program to be executed by this dedicated processor.



A single-chip solution for board-level BIST may be achieved by simultaneously generating the personality file of the ROM containing the test program.