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On Improving IEEE 1149.1 Reliability for On-Line Scan Operations

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Abstract

The IEEE 1149.1 standard provides no way to verify the integrity and correctness of scanned data, which may be acceptable for off-line operations but is a dangerous feature when concerning on-line processes. We need to have confidence in the string entering or leaving the target IC and our proposal is to allow the BST-controller read the parity of this string immediately after the scan operation: in case of error, it will be repeated. Only the four std BST-lines are required and no extra sates or Test Access Port control cycles are required.

Keywords: On-line test, BST, DFT, Dependable VLSI.

Introduction

The BST infrastructure [1] was designed for off-line tests mainly and, in this condition, the circuit under test has usually no activity during the scan operation, which will run smoothly and noise is a minor concern. However, the 1149.1 std is now an interesting vehicle for *on-line* test processes [2, 3, 4, 5, 6] and, particularly in concurrent operation, the circuit under test may induce noise which degrades the reliability of scan data. Other reasons to impact scan operation are the increasing TCK frequencies and lower operating voltages.

In most cases, the BST data is not targeted for an immediate action on the operation of the circuit under test, or it is read back to the BST controller and the probability of scan errors is not critical. This is true mainly if no instructions are loaded into the Instruction Register and the boundary scan cells are in the observability mode only. In case of error, there is (probably) enough time to repeat the scan operation, read the scan data again and check the results.

It must be pointed that, even in a standard off-line scan operation, errors may result from faults in the circuit under test or from scan errors. The worst case, however, are two situations in which the error is critical and we have no control on the consequences:

1. When scanning instructions to the Test Access Port, data misinterpretation may lead to the storage of an erroneous IR instruction, driving the BST cells to *controllability* modes which may impact the mission circuit operation.

2. In recent proposals for ICs tolerating faults, an enhanced boundary-scan infrastructure provides additional information to the target IC, under the control of the on-board BST-controller. The boundary-scan infrastructure is reused to monitor the circuit under test [7] and also to provide *decisions*, disabling the faulty circuit under test in a two-circuit architecture, aiming ICs which are able to tolerate permanent faults [8]. This architecture is named **XMR**, which stands for an *incomplete-TMR* architecture.

Once the BST data has immediate action here, we need feed-back on the integrity of the scan bits entering the target IC. This kind of problems was already addressed in [9], to increase the reliability of scan operations to the Test Access Port. However, this proposal needs an Interrupt scheme, puts some restrictions to the parity bit value and to the size of the strings for the Instruction Register. Furthermore, with an additional line (TINT), this solution is hardly compliant to the 1149.1 std. and the logic to handle and control an Interrupt infrastructure is probably more complex than the boundary-scan controller required in our approach, which is a simple state machine.

The Parity Generation Scheme

In the proposed scheme, the mission circuit (or IC) is seen as a group of testable Functional Blocks, each one bounded by a user defined scan register, as shown in figure.1. Each one of these chains is treated as the boundary scan register, and our main interest are the scan operations to the IC, aiming a fast response to avoid store erroneous data. Since we need not to change the Test Access Port instructions during circuit operation our first target are data scan operations (DR), but the same principle can be applied to the instruction register (IR) with no changes.

The parity of the incoming string will be calculated on-line, stored in a latch inside the target IC, and provided through TDO just after the last bit scanned. This way, the boundary-scan controller may know the parity of the data received into the target IC, in the TCK clock cycle immediately after the last bit sent and may repeat the scan cycle in case of error. This process is always the same, independently of being data and instruction scan operations.

Finally, the parity bit will be checked against the expected value, which can be calculated on-line in the boundary-scan controller, or stored together with the test patterns.

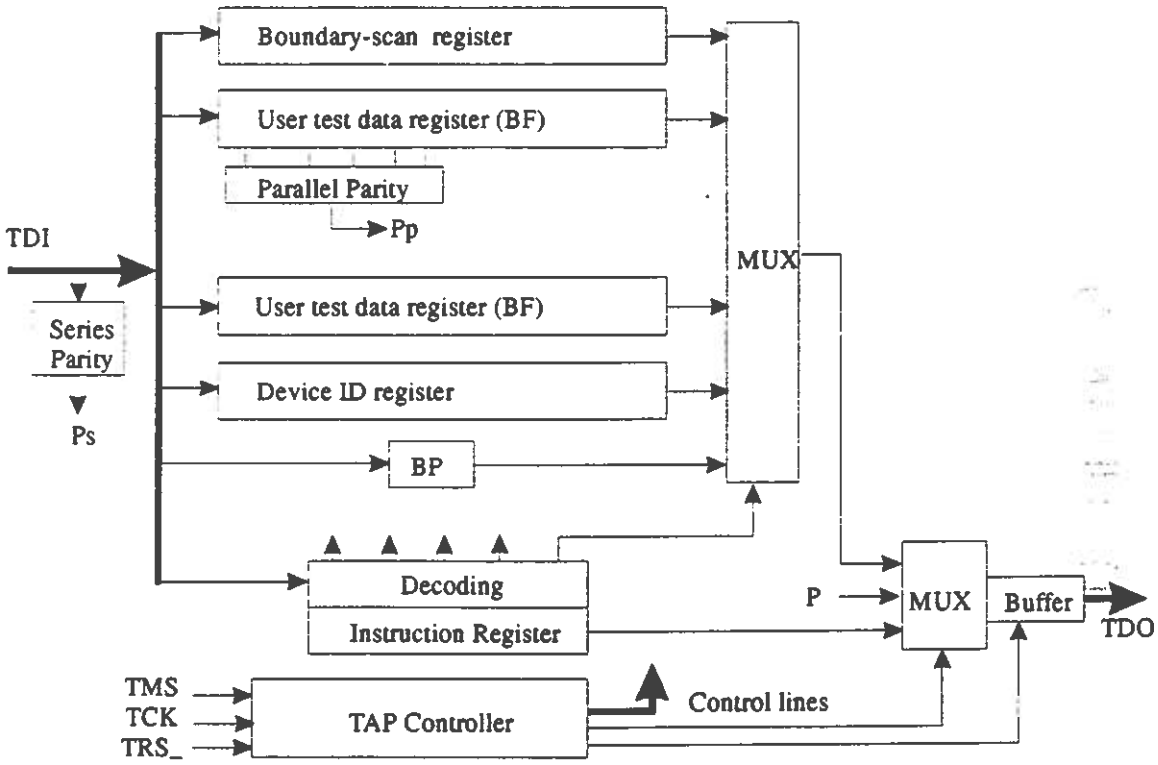

Figure 0-1. Alternative Parity generation circuits

As we can see in this figure, the parity signal can be generated inside the target IC through a *series* or *parallel* process. In the first case, the TDI line will by read as soon as the bits are received and the Ps signal will be generated and stored in a latch. In the second case, the Pp signal will be generated from the new values in the scan cells, allowing a higher degree of reliability but needs a parity generator for every user scan-chain and a multiplexer for all these parity lines.

It must be noticed that, in the parallel generation scheme, not all the cells in the register are required to generate the parity. In most cases only the cells which are loaded through TDI must be checked and this value is about one half of the cells in the chain.

The first case allows a very simple hardware, and is preferable if the probability of errors inside the IC can be neglected, but in both cases the Parity signal (Ps or Pp) will be ready at the same time and will be scanned out through the P line in the TDO multiplexer just after the last bit sent, as represented in figure.2. We can see the last scan bit sent ending at 1,50µs and followed by the parity bit (which starts in this moment), is expected to be read at 1.55µs and ends at 1,6µs.

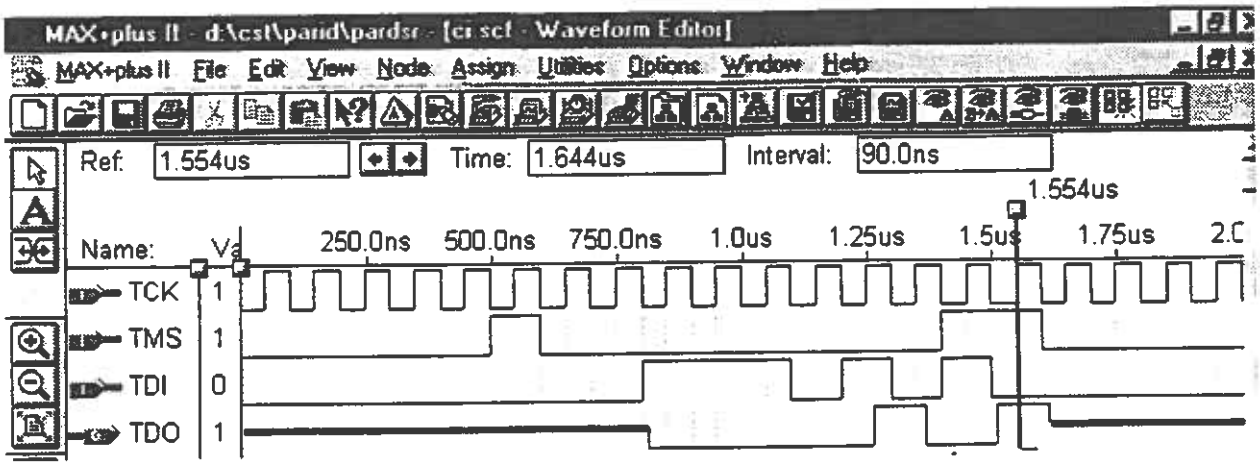

Figure 0-2. Time diagram simulation of a real circuit

The TAP Control Scheme

The state diagram for Test Access Port operation in the IEEE 1149.1 BST std, defines that in normal operation the last scan bit is transferred when the Test Access Port goes from state Shift to state Exit1: after this sate, TDO is expected to remain in high-impedance. Our proposal is to provide the parity bit in the Exit1 state. In the first, and more common case, the TAP controller will go into the Update state as shown in the figure.3.

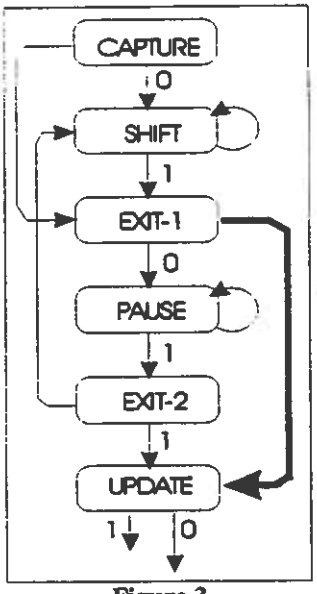

Figure.3

Obviously, in this case the new data will be stored, either good or bad, because the Test Access Port goes directly to the Update-DR (or IR) state. The solution to this problem is to provide the parity bit in the Exit1 state also, but go to the Pause state as shown in figure.4.

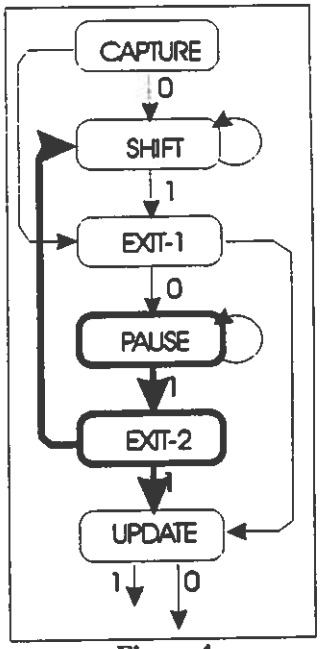

Figure.4

Now, the boundary scan controller may check the parity in this state and proceed to Exit2 and Update if there is no error, otherwise it will return to the Shift state and repeat the scan operation again.

Final comments

A small modification to the Test Access Port controller allows to read back the parity of the string received in the target IC, in order to verify scan data integrity. This means almost no hardware overhead but the parity generator and an additional input to the TDO multiplexer. The proposal, which requires no extra states or scan cycles, is non compliant to the 1149.1 std during a single TCK cycle only but, since in normal operation, there is no reason to stop the TAP controller in the Exit1 state, this change will not be detected by other compliant circuits. So, the advantages are much more important than the formal incompatibility and the advantages are:

- No impact on the mission circuit performance.
- Allows standard and simplified boundary-scan cells with no changes.
- Minimum overhead to the BST infrastructure: less than 1% to the std.

Finally we must notice that the user, or the boundary scan controller more precisely, are free to consider or not the parity bit, which is available in a transparent way.

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