## Adding Fast Parity Check to BST for Concurrent Monitoring

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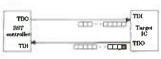
## Motivation

- The IEEE 1149.1 infrastructure is becoming increasingly reused during circuit operation (e.g. to increase dependability through concurrent monitoring)
- Pushing TCK frequencies and lowering voltages impact scan operations
- Scan-data reliability must be improved to cope with on-line operation requirements

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## The Proposal

- · To check the Parity of transmitted data
  - For each vector shifted into each BS IC, n+1 bits are read by the BST controller
  - The (n+1)th bit represents the parity of the data and will be checked be the BST controller



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Process BS register

Parity Generation

Parallel
Series

Checks final data inside scan cells
Detects internal and external errors
Overhead is higher

Process BS register

Process BS register

Process BS register

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Option 1

(parallel or series)

Shift → Exit\_1 → Update ...

No extra clock cycles are required, but...

Erroneous data will be stored before correction

Shift Exit-1 Update

TCK

Leat bit Parity Check to 1837 for concurrent monitoring European Test Workshop 1898

Capture

Shift Exit-1

Last bit Parity High 3

Adding Fast Parity Check to BST for concurrent monitoring European Test Workshop 1999 Capture Option 2 Shift (parallel or series) • Shift  $\rightarrow$  Exit\_1  $\rightarrow$  Pause  $\rightarrow$  $Exit_2 \rightarrow Update (or Shift) ...$ Pauso - Extra clock cycles are required, Exit-2 Update - In case of error, data will not be stored Shift Exit-! Pause Exit-2 Update Shift Exit-1 Pause Exit-2 Shift (correctly seamned data) (incorrectly scanned data)

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## Conclusion

- Capability to check the parity of every scan operation means higher reliability
- · Pros and cons:
  - Physical overhead: less than 1% of the BST infrastructure
  - Dynamic overhead:
    - · None with option 1
    - Two TCK cycles with option 2
  - Drawback: violates the High-Z rule for Exit-1

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