Adding Fast Parity Check to BST for Concurrent Monitoring

Jose M. Vieira dos Santos - ISEP / DEE

(jmvs@dee.isep.ipp.pt)

J. M. Martins Ferreira - FEUP / DEEC

(jmf@fe.up.pt)

Porto - **Portugal**

ETW,99

Motivation

- The IEEE 1149.1 infrastructure is becoming increasingly reused during circuit operation (e.g. to increase dependability through concurrent monitoring)
- Pushing TCK frequencies and lowering voltages impact scan operations
- Scan-data reliability must be improved to cope with on-line operation requirements

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The Proposal

- To check the Parity of transmitted data
  - For each vector shifted into each BS IC, n+1 bits are read by the BST controller
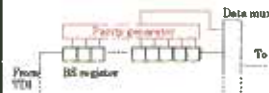 - The (n+1)th bit represents the parity of the data and will be checked be the BST controller
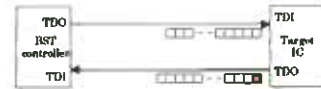
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Parity Generation

Parallel

- Checks final data inside scan cells
  - Detects internal and external errors
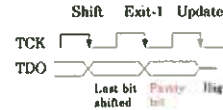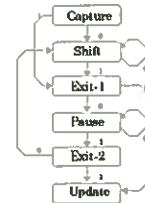 - Overhead is higher

Series

- Checks all data scanned through TDI pin
  - Detects external errors only
  - Small overhead

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Option 1
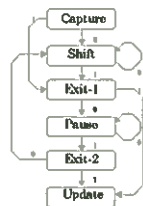(parallel or series)

- Shift → Exit_1 → Update ...
  - No extra clock cycles are required, but...
  - Erroneous data will be stored before correction

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Option 2
(parallel or series)

- Shift → Exit_1 → Pause → Exit_2 → Update (or Shift) ...
  - Extra clock cycles are required, but...
  - In case of error, data will not be stored

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Conclusion

- Capability to check the parity of every scan operation means higher reliability
- Pros and cons:
  - Physical overhead: less than 1% of the BST infrastructure
  - Dynamic overhead:
    - None with option 1
    - Two TCK cycles with option 2
  - Drawback: violates the High-Z rule for Exit-1

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