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Using the BS register for capturing and storing n-bit sequences in real-time

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Abstract

Boundary Scan Test is now widely accepted and used for the structural test of Printed Circuit Boards. However, the more demanding requirements of prototype debug and validation are not sufficiently covered by the mandatory and optional operating modes described in the IEEE 1149.1 Standard. Previous work has focused on this problem, having resulted in a new set of user-defined optional instructions addressing the use of the BS register to store in real-time a sequence of contiguous vectors, captured at its parallel inputs without / until / after a certain condition is found. In this paper we describe the tradeoff between input channels and storage capacity, by proposing a new operating mode where the BS register is used to capture / store an n-bit sequence captured at one single functional pin. We also describe how this operating mode can be further extended into the P1149.4 domain, for capturing / storing the n-bit data stream generated by a $\Sigma\Delta$ converter placed in the TBIC.

1. Introduction

Boundary Scan Test (BST) [1] is now widely accepted and used for the structural test of Printed Circuit Boards (PCB). Testing a board through its BST infrastructure proceeds in three main steps, which consist of testing the BST infrastructure itself, testing the interconnects among the components (including those buried into non-BST clusters), and testing the components (mainly through the activation of component-level BIST functions). Other advantages of using BST include simple test interface, assistance on functional debug and test, and availability during field operation debugging [2, 3, 4, 5]. However, the more demanding requirements of prototype debug and validation are not yet sufficiently covered by the mandatory and optional operating modes described in the IEEE 1149.1 Standard. This is especially true when debugging problems that only occur when the system under test is working in real-time, at its full operating speed [6, 7]. Traditionally, logic analysers are used (both as timing and state analysers) for debugging this sort of problems. In this paper, we propose the use of the BS register for capturing / storing an n-bit sequence, captured at one single functional pin, thus acting similarly to an one-channel timing analyser.

This paper is organised as follows: Section 2 presents and discusses previous work in this area, and the motivations that led to our current proposal. Section 3 describes how the BS register can be used to fulfil this new operating mode, activated by a user-defined optional instruction. Section 4 explains how this operating mode can be further extended into the P1149.4 domain, for capturing / storing the n-bit data stream generated by a $\Sigma\Delta$ converter placed in the TBIC. This 1-bit A/D converter is used, together with the capacities enabled by the TBIC, and ABM, control and switching structures, for converting the values present at any analog pin of components supporting both the IEEE P1149.4 test infrastructure and the proposed operating mode. Finally, section 5 concludes this paper with the final remarks and future work.

2. Background and motivation

Extending the use of BST for prototype debug and validation has already been proposed and analysed in several previous works, either in the form of adding new operating modes to this test technology or by adding new components with enhanced test functions to the system under debugging [8, 9, 10]. The case of embedded core-based systems has also been covered, by using the electronic access provided by this test infrastructure [11]. The concept of Design-for-Debug-and-Test (DfDT), in correspondence to the concept of Design-for-Testability (DfT), has also led to some variations or new optional operating modes for the BST infrastructure [12]. In this previous work, we have proposed, analysed, and implemented a new set of optional instructions that place the BST circuitry in special operating modes addressing the following debugging routines:

- Detect in real-time a breakpoint condition referring to the values present at the BS register PIs.
- Capture / store in real-time, in the BS register, a sequence of two contiguous vectors.
- Capture / store in real-time, in the BS register, a sequence of two contiguous vectors, until a certain condition is found.
- Capture / store in real-time, in the BS register, a sequence of two contiguous vectors, after a certain condition is found.

By trading off the number of input channels (PI of all BS cells) by storage capacity (total number of BS cells) it is possible to implement a one-channel timing analyser with a n-bit storage capacity, where n denotes the total number of BS cells in the device. While the input channel, referring to the BS cell PI, receives digital values, it is possible to use this same mechanism

to capture / store the values present in any analog pin, if a 1-bit $\Sigma\Delta$ converter is used to convert the analog values into digital ones. With this in mind, we proposed ourselves to develop a new operating mode for the BST infrastructure that could implement this functionality, both for digital and mixed-signal devices.

3. Capturing / storing n-bit sequences from a single pin

The goal of this new optional operating mode consists of using the BS register to capture and store, in real-time, an n-bit sequence corresponding to the values captured at one functional pin. This mode is selected by a user-defined optional instruction, named Memorise Sequence from Single Pin (MSEQ1P, in the abbreviated form). The pin that captures the values is selected by another user-defined optional instruction, named Select Pin (SELPIN, in the abbreviated form), which places an additional test data register in the TDI-TDO path, with a number of cells equal to the logarithm, in the basis 2, of the total number of BS register cells. The vector that identifies the position of the BS cell associated with the selected pin is shifted into this additional register, named Selected Pin (SP) register.

3.1 Sequence of steps

To capture / store an n-bit sequence it is necessary to perform the following steps:
- Shift in the SELPIN instruction in order to place the SP register in the device TDI-TDO path.
- Shift in the combination that selects the BS cell associated with the pin acting as the input channel. The order of the associated BS cell may be found in the device BSDL file (or data sheet). Usually, the BS cell closest to TDO is identified as BS cell [0] or cell$_0$.
- Shift in the MSEQ1P instruction, that will start the capture / store activity immediately after the TAP controller enters the Run-Test/Idle state. The captured values are stored in the BS register, which is currently selected by this optional instruction. The samples are stored in the capture / shift stage, by shifting them in a continuous loop, with the BS register acting as a circular buffer, as illustrated in Figure 7. The last sample (e.g., the most recent one) is always stored in the BS cell associated with the selected pin, while the first sample (e.g., the least recent one) is always stored in the BS cell that stands at the left of the previous one (assuming that BS cell [0] is the rightmost one and that BS cell [n-1] is the leftmost one). Notice that if the selected pin corresponds to BS cell [n-1], then the one that stands closer at the left side will be BS cell [0], as the BS register should be regarded as a circular buffer.
- To read out the stored sequence, place TAP controller in Shift-DR state, and apply cycles on TCK until the BS register contents are all shifted out. When MSEQ1P is active and the TAP controller moves through Capture-DR the BS register contents do not change.

3.2 Modifications in the group of test data registers and in the BS cell structure

The group of test data registers of the device now includes the SP register, as illustrated in Figure 1. In order to implement the functionality associated with this operating mode, the BS cell structure has to be slightly modified, as illustrated in Figure 2. Notice that this modification is minor, a new two-input AND gate in every BS cell. The output of this gate acts as the control signal of the multiplexer that feeds the capture / shift stage. The input signals are Shift (which acts as the multiplexer control signal in 'normal' BS cells e.g., as illustrated in [1, page 1-4]) and the line that comes from the m to 2^m decoder illustrated in Figure 8. This decoder decodes the SP register contents in order to allow the BS cell associated with the selected pin to capture the values present at its Parallel Input (PI) while the remaining cells shift the value present at their Scan Input (SI). The decoder output lines are active low so that a logic '0' forces the AND result to be false (or low), causing the multiplexer upper branch (PI) to be selected. A logic '1' in the decoder output line causes the AND result to be controlled by the Shift signal. The decoder truth table presented in Table 1 helps the reader to understand its behaviour. The decoder is enabled when the TAP controller is in Run-Test/Idle and MSEQ1P is active. When not enabled, all output lines are at logic '1', thus not interfering with the result of the additional AND gate. This way the Shift signal gains full control over the multiplexer, as in a 'normal' BS cell, thus guaranteeing the same behaviour for the three mandatory instructions (BYPASS, SAMPLE / PRELOAD and EXTEST).

While this modification is minor, an additional one is needed in BS cell [n-1] (closest to TDI), to implement the circular buffer. The structure illustrated in Figure 3 refers exclusively to this BS cell, where it can be seen that an additional multiplexer was added in order to allow the selection between TDI and the Scan Output (SO) from BS cell [0] (thus implementing the circular buffer). When MSEQ1P is active and the TAP controller is in Run-Test/Idle the multiplexer output is connected to the BS cell [0] SO. In all other conditions, TDI will be selected. The multiplexer that feeds the capture / shift stage acts in the previously described way. If BS cell [n-1] is selected (decoder line at logic '0'), the values present at its PI will be captured and shifted along the BS register (notice that all other BS cells are used to store the captured sequence). If BS cell [n-1] is not selected (decoder line at logic '1') the values present at the SI will be captured and shifted along the BS register (until they reach the BS cell that stands immediately at the left side of the currently selected one). If the decoder is not enabled (MSEQ1P·Run-Test/Idle = false), TDI is selected as the SI of BS cell [n-1], and the Shift signal controls the multiplexer that feeds the capture / shift stage of this and all other BS cells.
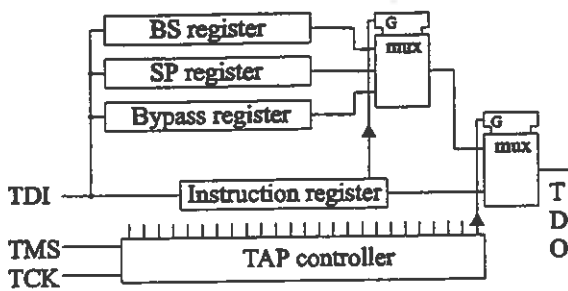
Figure 1: The group of test data registers after implementing the *SELPIN* optional instruction.
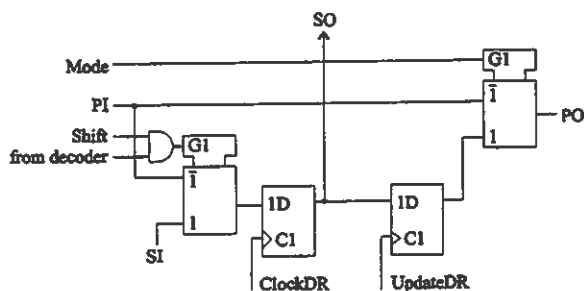

Figure 2: Modified BS cells able to support the *MSEQIP* optional instruction.

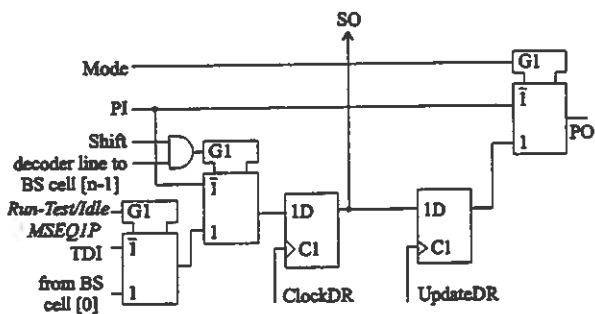| en	SP	cell$_{n-1}$	cell$_{n-2}$	Other cells	cell$_1$	cell$_0$
0	X	1	1	all '1s'	1	1
1	0	1	1	all '1s'	1	0
1	1	1	1	all '1s'	0	1
1	...	1	1	...	1	1
1	n-2	1	0	all '1s'	1	1
1	n-1	0	1	all '1s'	1	1

Table 1: Truth table of the m to 2^m decoder.

Figure 3: BS cell closest to TDI, modified in order to support the *MSEQIP* optional instruction.

3.3 Modifications in the BS cell control signals

The modifications in the BS cell control signals are summarised in Table 3. The 1st column contains the control signals, the 2nd column presents the corresponding logic equation, for a BS cell able to implement the functionality associated with the three mandatory instructions, according to what is described in [1, chapter 5], and the 3rd column presents the new

logic equations. Notice that UpdateDR and Mode hold the same logic equation, while Shift now includes the *Run-Test/Idle* state (the actions related to *MSEQIP* occur while the TAP controller is in this state), and ClockDR is expanded in order to accommodate the two actions required by *MSEQIP* – not capture in the *Capture-DR* state, and capture in the *Run-Test/Idle* state.

3.4 Questions to be addressed

Some questions naturally arise from the previous description. This section tries to answer some of them:

• The SP register does not need an update stage, as the possible intermediate values resulting from the shift process will not cause any misbehaviour. The clock signal of this simple shift register (without parallel load) is active when *SELPIN* is active and the TAP controller is in *Shift-DR*.

• Changing the values present in the BS register, during *Run-Test/Idle* (with *MSEQIP* active) is allowed by the IEEE 1149.1 Standard [1, page 5-3[1]].

• Holding the values present in the BS register, during *Capture-DR* (with *MSEQIP* active) is allowed by the IEEE 1149.1 Standard [1, page 5-4[2]].

4. Sigma-Delta ($\Sigma\Delta$) conversion in analog pins and store of n-bit sequences

The optional operating mode presented in the previous section may also be employed in mixed-signal devices that conform to the IEEE P1149.4 proposal to standard [13]. As the TBIC and ABM control structures require 4 BS cells, each, the total number of cells in the BS register of a mixed-signal device will exceed that of a pure digital one, if the number of bidirectional pins is approximately the same. This large storing capacity may favour the use of the proposed optional operating mode, which consists of implementing a Sigma-Delta ($\Sigma\Delta$) converter within the TBIC switching structure. Using the converter illustrated in

Figure 4, the device internal test bus, and both the TBIC and the ABM, control and switching structure, it is possible to capture and store in the BS register the data stream resulting from the A/D conversion. The sampling rate may match the maximum TCK frequency accepted by the device, while the digital filter is placed outside for saving both silicon area and power consumption. Notice that this part of the $\Sigma\Delta$ converter may be responsible by as much as 75% of the total area, and for the major part of the total power consumption [14]. Splitting the $\Sigma\Delta$ converter into its 1st order modulator (implemented within the device) and its digital filter (outside) allows a straightforward implementation of the proposed operating mode. The data stream generated by

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[1] "... In *Run-Test/Idle*, activity in selected test logic occurs only when certain instructions are present."
[2] "... if capturing is not required for the selected test, then the register retains its previous state unchanged."

the 1st order modulator is captured by the CALIBRATE cell of the TBIC control structure, and shifted / stored along the remaining cells of the BS register. This solution however implies a delay between the moment the samples are captured / stored and the moment they are fed into the digital filter, due to the read out process that takes place only when the TAP controller is in *Shift-DR* (where the BS register contents may be shifted out). The implementation of this operating mode is simplified if the control structure of the TBIC, specifically the CALIBRATE cell, is always placed closest to TDI. This way there is no need for a decoder to identify / select this cell, and the all length of the BS register may then be used to store the n-bit sequence generated by the 1st order modulator.
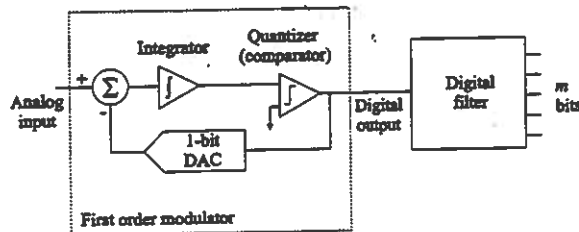
Figure 4: First order $\Sigma\Delta$ ADC block diagram.

4.1 Sequence of steps

To capture / store the n-bit sequence generated by the 1st order modulator it is necessary to perform the following steps:
- Shift in the $\Sigma\Delta$ Conversion from one Pin ($\Sigma\Delta C1P$, in the abbreviated form) optional instruction that places the BS register in the device TDI-TDO path.
- Place the TAP controller in *Shift-DR* and shift in the vector that selects the following combination:
  - Connect the selected analog pin, which values are to be converted, to the AB2 line, through switch SB2. Switch SD closed and remaining switches open, as illustrated in Figure 5. Notice that the selected combination is non-intrusive, which allows the pin to carry out its normal function. In all other ABM associated with analog pins, switch SD closed and remaining switches open. The values shifted to all DBM are irrelevant.
- Place the TAP controller in *Run-Test/Idle*. While the TAP controller is in this state and $\Sigma\Delta C1P$ is active, the CALIBRATE cell (that is part of the control structure of the TBIC) captures in the TCK rising edge the value present at the digital output of the 1st order modulator. The remaining BS cells (from the TBIC and ABM control structures, plus the DBM) are in shift mode.
- To read out the stored sequence, place the TAP controller in the *Shift-DR* state, and apply cycles on TCK until the BS register contents are all shifted out. When $\Sigma\Delta C1P$ is active and the TAP controller moves through *Capture-DR* the BS register contents do not change. The n-bit sequence generated by the modulator should then pass through the external digital filter.
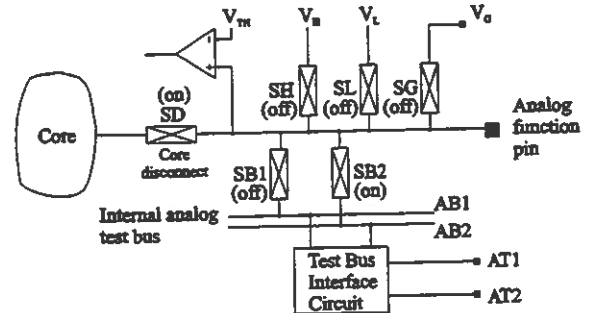
Figure 5: ABM switching structure, showing the switch conditions for the selected analog pin.

4.2 Modifications in the TBIC switching and control structures

In order to support this new operating mode, it is necessary to implement the 1st order modulator in the TBIC switching structure, and connect its digital output to the multiplexer that feeds the CALIBRATE cell of the TBIC control structure. The control signal of this multiplexer is now generated by a logical AND between the ShiftDR signal (the formerly control signal) and a new signal active low when both the TAP controller is in *Run-Test/Idle* and $\Sigma\Delta C1P$ is active. These modifications are illustrated in Figure 6 and in Figure 9, respectively.
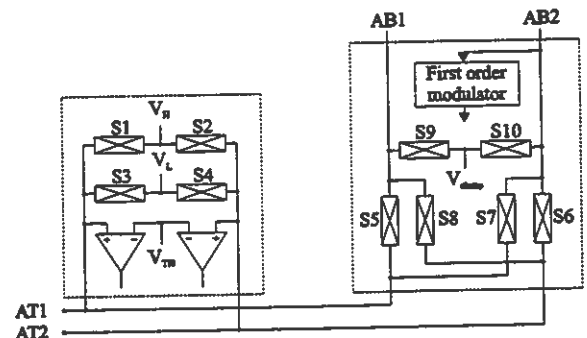
Figure 6: Placing the 1st order $\Sigma\Delta$ modulator into the TBIC switching structure.

4.3 Modifications in the TBIC and ABM switching patterns, and BS cell control signals

To support the $\Sigma\Delta C1P$ instruction it is needed a new switching pattern for the TBIC and some modifications in the ShiftDR and ClockDR control signals that feed all BS cells. All other control signals are identical to the ones used in a device that implements the four mandatory instructions (includes now the mandatory *PROBE* instruction) Regarding the ABM switching structure it is possible to reuse one of the existing switching patterns. The new switching pattern specifies that only the AB1 line is clamped through switch S9. The remaining switches of the TBIC should be open.

The state of all these switches is described in Table 2, using the format that appears on [13]. The new switching pattern does not depend upon the values present in the update register of the TBIC control structure, but rather on the active instruction, in this case the $\Sigma\Delta CIP$ optional instruction. As for the ABM, the switching pattern 17 [13, page 66] should be used on the selected analog pin, while using switching pattern 16 for the remaining analog pins. Table 4 summarises the logic equation for the control signals of all BS cells, before and after implementing the $\Sigma\Delta CIP$ instruction.

Pat.	Switch conditions										Connections
	1	2	3	4	5	6	7	8	9	10	and function
P10	0	0	0	0	0	0	0	0	1	0	AB1/2 disconnected from AT1/2. AB1 clamped.

Table 2: Additional switching pattern for the TBIC, in order to support the $\Sigma\Delta CIP$ optional instruction.

4.4 Questions to be addressed

Changing the values present in the BS register, during *Run-Test/Idle*, and holding the values present in this same register, during *Capture-DR* (with $\Sigma\Delta CIP$ active), is allowed by P1149.4 [13, page 22[3]]. The new switching pattern results in an overhead in the logic block that decodes the current instruction.

5. Conclusion

In this paper we proposed and described a new optional operating mode for the BS test infrastructure. This proposal results from an extension of a previous work, regarding the use of this test technology for prototype debug and validation. The proposed operating mode consists of using the BS register (namely the capture / shift stage) to store the values captured at one single functional pin, by means of its associated BS cell. The BS register is configured as a circular buffer though an additional multiplexer placed at the BS cell closest to TDI. Additional hardware includes a two-input AND gate for every BS cell, an m to 2^m decoder and the SP register that contains the position of the selected pin. Notice that this additional circuitry allows any BS cell to be selected as the input-channel of the capture / stored n-bit sequence. This operating mode also implies some modifications in the logic equations of the control signals feeding the BS register, although these modifications do not violate any rule stated in the 1149.1 Std. The extension into the P1149.4 domain was also considered, leading to a similar operating mode. In this case, the BS register is used to store the n-bit data stream generated by a $\Sigma\Delta$ converter (more specifically, its 1st order modulator) implemented within the TBIC of

the device. The analog input of the 1st order modulator may be connected to any analog pin within the device, using that capacities enabled by the ABM control and switching structures. The stored sequence has to be read out in order to feed the external digital filter, thus causing a delay between these two moments (capture and filtering). The overhead associated with this operating mode includes a single two-input AND gate in the TBIC control structure (if the CALIBRATE cell is placed closest to TDI), the 1st order modulator, and the new logic equations for the control signals of the BS register. Again, the modifications associated with these signals do not violate any rule in the P1149.4, although a new switching pattern is needed for the TBIC switching structure. This new optional operating mode will now be implemented in a prototype device currently used to validate the work described in [12].

6. References

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[3] "... The interpretation of the rules governing those structures and facilities that are common to this standard and to IEEE Std 1149.1 shall be determined by IEEE Std 1149.1."
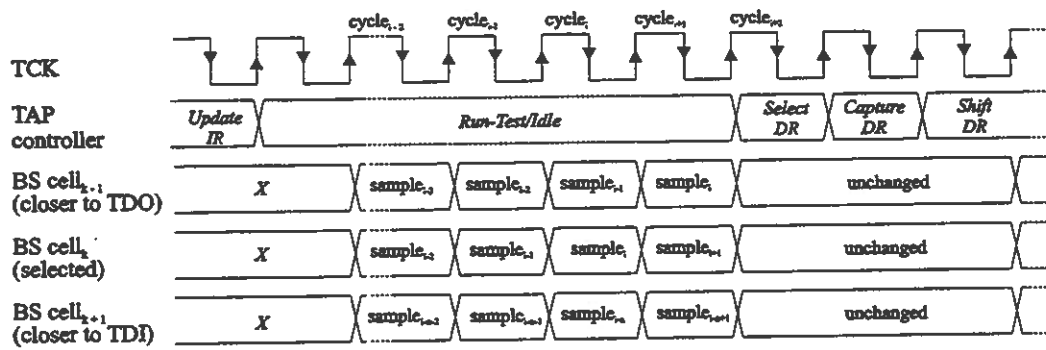
Figure 7: Time diagram of capturing / storing an n-bit sequence in the BS register.
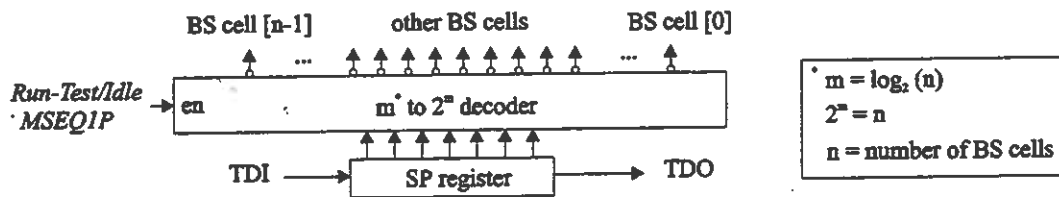

$$m = \log_2 (n)$$
$$2^m = n$$
n = number of BS cells

Figure 8: Decoder (m to 2^m) that identifies the BS cell associated with the selected pin.
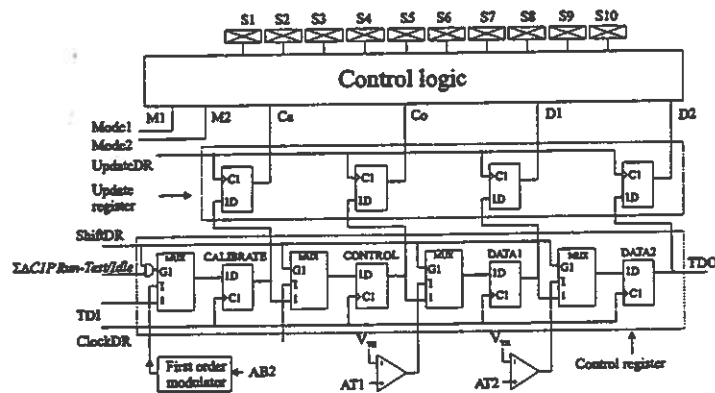

Figure 9: TBIC - Example implementation of the control structure supporting the $\Sigma\Delta C1P$ optional instruction.

Signal	Mandatory instructions	Support of $MSEQ1P$ optional instruction
UpdateDR	!TCK·Update-DR	Identical
ClockDR	TCK·(Shift-DR + Capture-DR)	TCK·(Shift-DR + Capture-DR·!MSEQ1P + Run-Test/Idle·MSEQ1P)
Shift	Shift-DR (registered)	Shift-DR + Run-Test/Idle (registered)
Mode	EXTEST	Identical

Table 3: Logic equations of the BS cell control signals before / after implementing the $MSEQ1P$ optional instruction[4].

Signal	Mandatory instructions	Support of $\Sigma\Delta C1P$ optional instruction
UpdateDR	!TCK·Update-DR	Identical
ClockDR	TCK·(Shift-DR + Capture-DR)	TCK·(Shift-DR + Capture-DR·!ΣΔC1P + Run-Test/Idle· ΣΔC1P)
ShiftDR	Shift-DR (registered)	Shift-DR + Run-Test/Idle (registered)
Mode	EXTEST	Identical
Mode1	Depends on current instruction	Identical
Mode2	Depends on current instruction	Identical

Table 4: Logic equations of the BS cell control signals before and after implementing the $\Sigma\Delta C1P$ optional instruction.

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[4] ! stands for NOT, · stands for AND, + stands for OR.