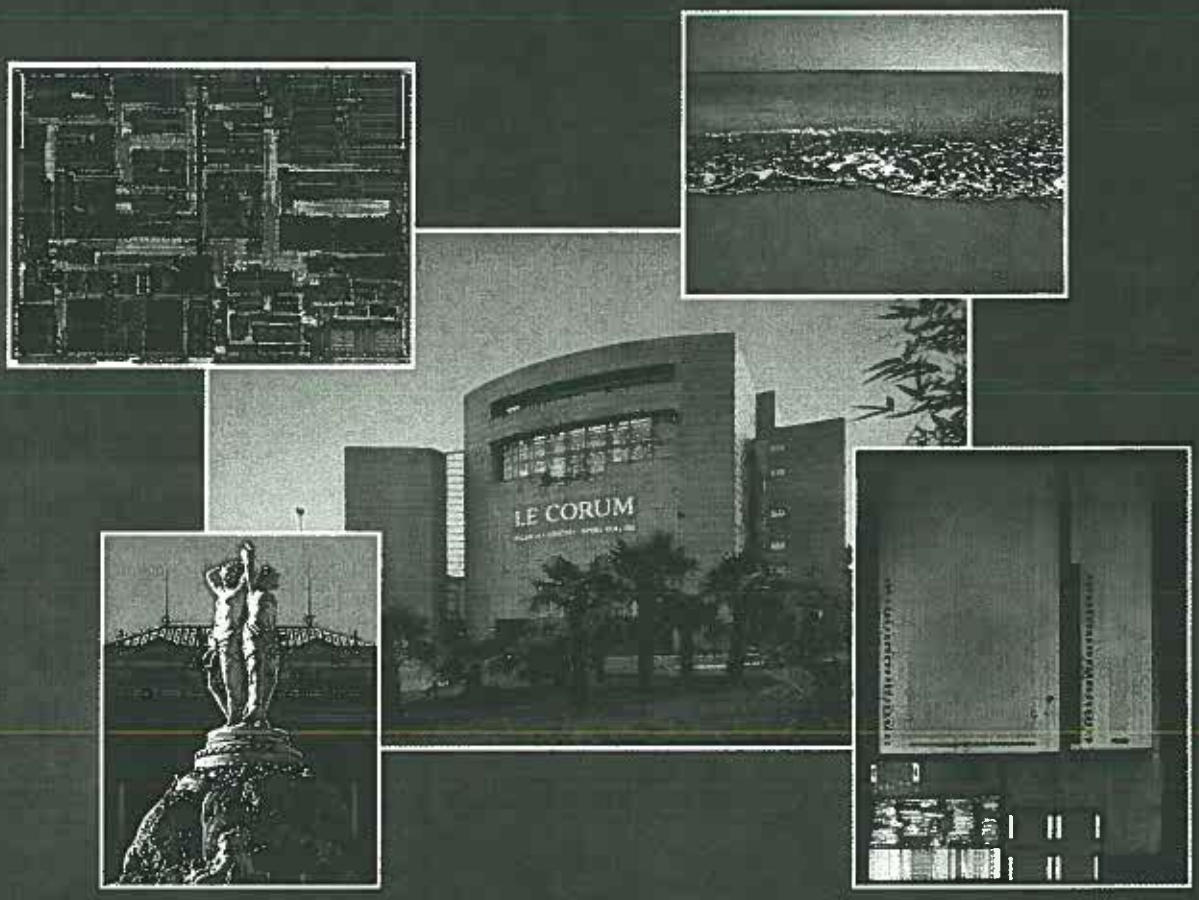
PROCEEDINGS OF

DCIS 2000



15th Design of Circuits and Integrated Systems Conference

Montpellier - Le Corum, France

November 21-24, 2000

LIRM

The RaT technique for concurrent test of dynamically reconfigurable hardware

Manuel G. Gericota[1], Gustavo R. Alves[1], José M. Ferreira[2]

[1]Department of Electrical Engineering
Instituto Superior de Engenharia do Porto
Rua Dr. António Bernardino de Almeida, 4200-072 Porto, Portugal
E-mail: (mgg,galves)@dee.isep.ipp.pt

[2]Department of Electrical and Computers Engineering
Faculdade de Engenharia da Universidade do Porto
Rua dos Bragas, 4050-123 Porto, Portugal
E-mail: jmf@fe.up.pt

Abstract

A new class of FPGAs that enable partial and dynamic reconfiguration has been recently introduced into the market, opening exciting possibilities for dynamically reconfigurable hardware systems. While enabling concurrent reconfiguration without disturbing system operation, this technology also raises a new test challenge: the reconfiguration process can activate faults which would otherwise not be visible. This paper proposes a structural concurrent test method that reuses the IEEE 1149.1 infrastructure, exploiting the same dynamic and partially reconfigurable features underlying this test challenge.

1. Introduction

Reconfigurable logic devices, namely FPGAs (Field Programmable Gate Arrays), experienced a considerable expansion in the last few years. These components enable savings in board space, quicker turn-around time and an unsurpassed degree of flexibility, when compared to traditional off-the--shelf LSI/VLSI components with pre-defined functionality. The advent of dynamic and partially reconfigurable SRAM-based FPGAs (e. g. the Virtex family from Xilinx), reinforced these advantages and added new possibilities by enabling the dynamic customisation of hardware functions to a particular system or application "on-the-fly" [1].

The need to reprogram the whole device, halting its operation (and consequently halting the operation of the circuit or system where they are inserted), is the main limitation associated with classic SRAM-based FPGAs. Additionally, the contents of all registers (state information) are lost when the component is reprogrammed. Manufacturers address these issues in new FPGA generations by supporting partial device reconfiguration, which can take place concurrently with the system operation and without destroying internal state information.

Dynamic reconfiguration goes beyond "in-system reprogramming", since it does not interrupt the operation of the device. However, the very high levels of integration and sub-micron technologies used in these FPGAs lead to a higher occurrence of defects [2], creating a critical need for fault tolerance features. High levels of reliability can only be achieved by continuously testing all FPGA blocks, in search of emerging defects that become visible in result of the reconfiguration process.

A novel structural concurrent test method is proposed in this paper, with very low test overhead, which reuses the new dynamic and partially reconfigurable features introduced by these devices and the well established boundary-scan (BS) test infrastructure [3] defined in the IEEE 1149.1 standard [4]. The proposed solution requires that the FPGAs used support partial dynamic reconfiguration through the 1149.1 TAP (Test Access Port), a feature which is possible in the Xilinx Virtex family, recently introduced in the market.

We start by considering a structural test solution for the Configurable Logic Blocks (CLBs) of an FPGA, without disrupting system operation, which is then followed by the presentation of the proposed functional replication method, and its integration in the BS infrastructure. A final section presents the directions for further research.

2. The RaT Freed Resources Technique

An FPGA device comprises an array of independent CLBs, surrounded by a periphery of Input/Output

Blocks (IOBs), which are interconnectable by configurable routing resources, as shown in figure 1.

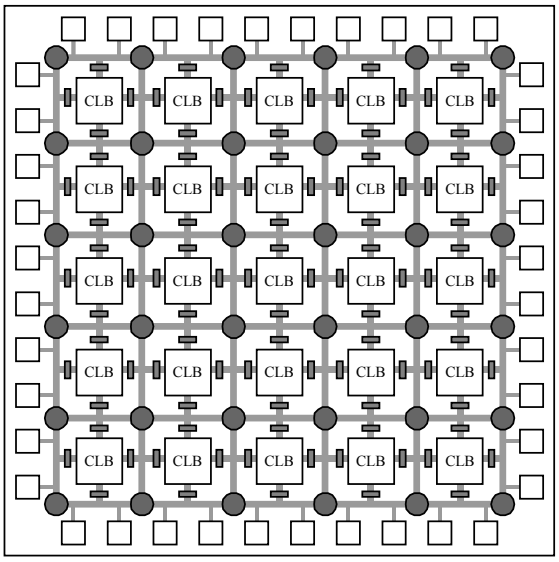


Fig. 1. Schematic representation of an FPGA.

In the vast majority of cases, only part of the FPGA resources are required to implement a given functional specification. Even in those cases where independent hardware blocks share the same FPGA device, with the aim of reducing board space, it is highly improbable that a 100% usage of the FPGA resources is achieved.

It is therefore possible to consider a test strategy whereby temporarily unused CLBs are released for test, without compromising the operation of the FPGA, while the remaining CLBs are requested and in use by the current implementation. Unused CLBs which have been successfully tested are available as spare parts, that may be used to replace other resources found to be defective. The solution proposed in this paper guarantees that the whole FPGA can be tested, without disturbing the system operation, provided that at least one unused CLB is available in the current implementation. Fault tolerance features will however require more than one unused CLB, since a pool of spare resources has to be continually available.

The proposed test method uses what we called the RaT (Replicate and Test) Freed Resources technique, represented in figure 2. This technique scans the whole set of CLBs, transferring an atomic subset of the current implementation to a previously unused CLB which has been successfully tested. This operation will in turn release the previously used CLB to be tested, and passed on to the pool of spare resources, in the event of a positive test outcome.

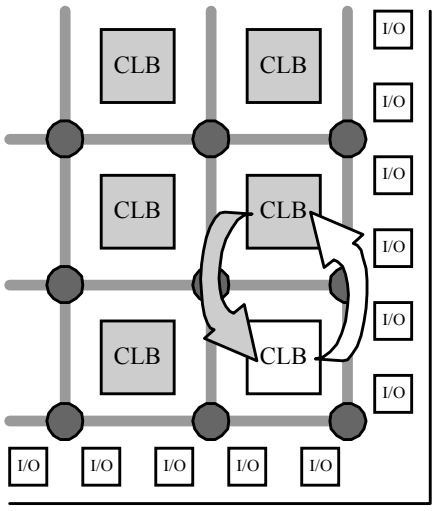


Fig. 2. CLB replication and rotation of freed resources.

The proposed method is only feasible in the case of those devices that support dynamic partial reconfiguration, so as to enable the replication of the CLB (functional and state information) and the re-establishment of the interconnections, without disrupting the operation of the device.

3. R(eplication)aT: the R part

Replication is not a trivial task, depending on the structure of the CLB to be tested and on the readback mechanism available, as well as on the functional specification currently implemented in the FPGA. If the current CLB function is purely combinational, there are no state (register) values to be copied during the replication process. However, and in the case of a CLB implementing a sequential function, the internal state information has to be preserved during the replication process.

As an example, in those FPGAs belonging to the recent Xilinx Virtex family, it is possible to read the value of a register, but not to perform a direct write operation. An alternative method to copy state information from one register to another therefore has to be implemented. The solution proposed in this paper creates a temporary transfer path between the two CLBs and copies state information by applying a clock pulse, synchronous with TCK (the 1149.1 test clock signal), as described in [5].

The Virtex family CLBs are of the Look-Up Table (LUT) type, which may be used to implement purely combinational functions or as distributed Random Access Memory (RAM) blocks. Since those bits written in the LUT are part of the configuration bit stream of the FPGA, the replication process starts with a readback operation. Reprogramming the LUT of the spare CLB then follows, together with the other configuration bits. If the LUT is used as RAM,

the readback operation may also be used to acquire the values currently present in each memory cell. No value should be written in the LUT while the readback and reprogramming operations take place, or otherwise a coherency problem will arise (since the values written in the spare CLB LUT will already be outdated, and those that were meanwhile written in the LUT of the CLB about to be released for test will be lost).
In order to minimise the usage of routing resources, replication is only performed between neighbouring CLBs (replication of more than one block at a time, or between blocks far from each other, might become impossible due to the scarcity of routing resources). Since all readback and reconfiguration operations are controlled through the BS infrastructure, the test overhead of the proposed method is very low (both at component and board levels).

4. RaT(est): the T part

Built-In Self-Test (BIST) structures previously proposed by several authors [5,6] require the allocation of significant resources. The necessary logic blocks, routing resources, and number of pins, represent a high test overhead, which is further aggravated due to the need to halt the system clock. Dynamic partial reconfiguration raises a new test challenge due to the possible occurrence of faults that become visible due to the reconfiguration process itself, but at the same time provides the necessary mechanisms to overcome the drawbacks inherent to the previous test methods. Test vector application and response capturing can be done through the BS infrastructure, reducing the test overhead of BIST techniques, while keeping all tests completely transparent to the user.
In order to test a CLB, a test configuration must first be defined, and then a set of test vectors generated and applied to its inputs. Depending on the CLB structure, multiple test configurations may be necessary to achieve 100% fault coverage, each with its own set of test vectors. To minimise the test application time, without compromising the fault coverage, each test configuration and the corresponding test vectors have to be carefully studied.
Since the reconfiguration time is higher than the test application time, a trade-off exists between the number of reconfiguration operations and the number of test vectors. The BS infrastructure is used for test vector application and response capturing, with the CLB outputs being routed to unused BS cells associated with the IOBs. Since all IOBs (bounded or unbounded) are considered as independent 3-state bidirectional pins in a single scan chain, three data register bits are provided per IOB, as shown in figure 3: input data, output data, and 3-state control. In practice many of these bits are redundant (depending on the pad configuration), but they are not removed from the scan chain.

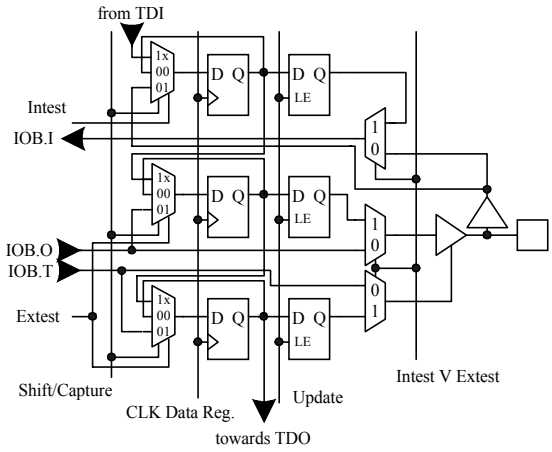


Fig. 3. BS cells per Virtex IOB [7].

Since redundant registers are used to capture the responses to the test vectors applied to the CLB under test, no extra resources are used for this purpose. The SAMPLE / PRELOAD instruction is used to capture the value present in each pad, into the corresponding BS register cell. This procedure is completely transparent to the system, contrary to what happens with the update operation, which is necessary to apply the test vectors to the CLB inputs (i.e. the “write” operation).
It is not possible to apply the test vectors through the BS register without affecting the values present at each FPGA input. The application of test vectors requires the BS cells to isolate the pins from the internal logic, preventing the normal operation of the system. It is however possible to overcome this problem by using a dedicated user register, since the Virtex FPGAs support up to two additional internal scan chains. The test vectors to be applied to the CLB under test are therefore shifted in through an user defined scan chain, without conflicting with the values present in the FPGA input pins (the scan chain length is equal to the number of inputs of each CLB). Since each Virtex CLB has a total of 15 inputs, and each CLB has four registers, four CLBs are used to implement the scan chain. The results are captured and shifted out through the BS register, in a way that is completely transparent to the operation of the FPGA.
Figure 4 illustrates the configuration of the FPGA while a CLB is being tested. Due to the need to minimise routing resources and other test overhead factors, a single CLB is tested at each time. Notice however that this process is continuously running in a background mode, meaning that speed is not a relevant requirement (provided that the whole FPGA

is tested in "real-time", as seen from the application point of view). Testing more than one FPGA CLB at a time would imply an extended use of routing resources (which might not be available), and the availability of a user register with a length equal to the number of inputs of each CLB, multiplied by the number of CLBs being tested simultaneously.

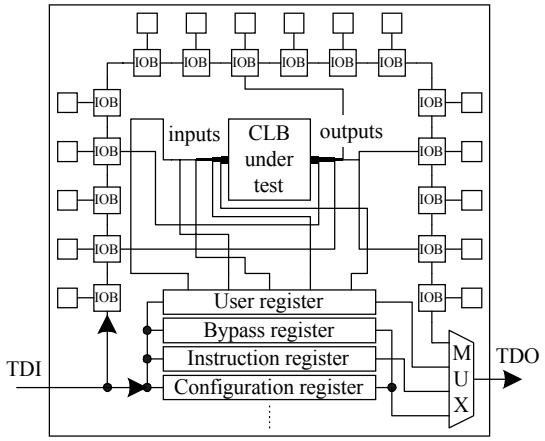


Fig. 4. Test of a CLB.

A list of faulty resources may be maintained, based on the information extracted from the test responses, so that future reconfigurations do not use defective CLBs. While requiring the existence of spare CLBs, this solution introduces fault tolerance features that greatly enhance system reliability.

5.Conclusion

The solution proposed in this paper enables the implementation of a concurrent test method that reuses the standard BS infrastructure and the novel partial dynamic reconfiguration features of recent FPGA devices, in order to improve the reliability of reconfigurable hardware systems, with minimal test overhead and in a way that is completely transparent to the system operation.

Experiments are currently under way with the objective of determining an optimal solution (test application time, fault coverage), in terms of the trade off between the number of reconfiguration operations and the number of test vectors. Later research work is also planned to address other FPGA resources, namely interconnections and RAM--blocks, again by reusing the BS infrastructure.

References

[1] C. Maxfield, "Logic that mutates while-u-wait", *EDN Magazine*, N.º 23, 7 November 1996.

[2] F. Hanchek, S. Dutt, "Methodologies for Toleranting Cell and Interconnect Faults in FPGAs", *IEEE Transactions on Computers*, Vol. 47, N.º 1, pp. 15-33, January 1998.

[3] C. Hamilton, G. Gibson, S. Wijesuriya, C. Stroud, "Enhanced BIST-Based Diagnosis of FPGAs via Boundary Scan Access", *Proceedings of the 17th IEEE VLSI Test Symposium*, Dana Point, California, pp. 413-418, 25-29 April, 1999.

[4] *A Standard Test Access Port and Boundary Scan Architecture* (IEEE Std 1149.1), IEEE Standards Board, May 1990.

[5] M. Abramovici, C. Stroud, S. Wijesuriya, C. Hamilton, V. Verma, "On-Line Testing and Diagnosis of FPGAs with Roving STARs", *Proceedings of the 5th IEEE International On-Line Testing Workshop*, Rhodes, Greece, pp. 2-7, 5-7 July 1999.

[6] N. Shnidman, H. Mangione-Smith, M Potkonjak, "Fault Scanner for Reconfigurable Logic", *Proceedings of the 17th Conf. on Advanced Research in VLSI*, Ann Arbor, Michigan, pp. 238-249, 15-16 September 1997.

[7] "Configuration and Readback of Virtex FPGAs Using (JTAG) Boundary-Scan", Xilinx Application Note 139, version 1.2, 18 February 2000 (available at http://www.xilinx.com).