SPICE Implementation of a Finite Element Method Based Model for Bipolar Power Semiconductors

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Abstract - This paper describes the methodology associated with the practical implementation, in *SPICE* circuit simulator, of a Finite Element Method (*FEM*) based model developed for Bipolar Power Semiconductor (*BPS*) simulation. The methodology is based on a modular approach that associates each zone of the semiconductor to a subcircuit implemented into *SPICE* simulator. Modeling a semiconductor is based on union of a set of subcircuit modules necessary for the different zones. Calculus of instantaneous distribution of lightly doped zones carriers (ambipolar diffusion equation (*ADE*) solution in space/time) is made of a group of subcircuit modules, analogue to *FEM* elements. The paper shows how each module is implemented and how easily elements with different sizes, topologies or physical properties are designed. Remaining semiconductor zones (highly doped emitters narrow base and *MOS* zones) are modeled with subcircuits using classical approaches. Voltage drops are modeled with subcircuits implementing a Boltzmann approach for junctions and a Poisson approach for depletion zones. Description for obtaining each associated *SPICE* subcircuit is presented. Global solution is approached by serial interconnection of these modules (each one directly related to one element of the domain). The paper concludes with simulation results showing hole/electron distribution, in time/space, in low-doped zones of *PIN* Diodes, *BJTs* and *IGBTs*, as well as, corresponding dynamic commutation waveforms for current and voltage.

1 Introduction

This paper presents practical implementation of a modeling method for *BPS*. The method is based on unidimensional approach that associates each zone of the semiconductor to a subcircuit capable of being implemented in any general circuit simulator (such as *SPICE*), in a modular mode[1].

Modeling of a semiconductor begins with identification of the different zones that constitute the device, such as, low doped, high doped and ohmic zones, narrow bases, junction and space charge and *MOS* zones. For large and lightly doped zones electron/hole time/space distribution is found solving *ADE* with *FEM* [2], [3], [4], [5]. Highly doped emitters are modeled as recombination sinks using *h* parameters as well as narrow bases with charge control principles. Ohmic zones use knowledge of time/space carrier concentration and junction drops Boltzmann approach, space charge uses Poisson equation and MOS part of the devices is represented through standard models [6], [7], [8], [9].

After identification of these zones we just use modules that emulate their behaviour and make connections between them using boundary conditions.

The paper is organized as it follows: Next section introduces circuits for *ADE* solution. Section 1 introduces circuits associated with solutions for narrow bases, high doped, ohmic, junction, space charge and *MOS* zones. Section 4 shows how to put together the obtained modules for power Diode, *BJT* and *IGBT* modeling. Finally Sections 5 and 6 present obtained results and conclusions.

2 *ADE* Circuit solver

ADE unidimensional solution of hole/electron distribution gives the following set of *ODEs*[1]:

$$[C]\left[\frac{\partial V}{\partial t}\right]+[G][V]+[I]=0 \quad (1)$$

These *ODEs* have an immediate electrical analogy with a circuit made of capacitors, resistors and controlled current sources. This electrical analogy is easily implemented as a series of elementary *RC* nets (Fig. 1) of the type:

$$[C(e)]\left[\frac{\partial V(e)}{\partial t}\right]+[G(e)][V(e)]+[I(e)]=0 \quad (2)$$

$$\text{with: } C(e)=M(e)=\int_{Ve}\frac{[N]^T[N]}{D}dV \quad (3)$$

$$G(e)=K(e)=\left[\int_{Ve}[B]^T[B]dV+\int_{Ve}\frac{[N]^T[N]dV}{D\tau}\right] \quad (4)$$

$$I(e)=F(e)=\int_{S_e}f(t)[N]^T dS_e-\int_{S_e}g(t)[N]^T dS_e \quad (5)$$

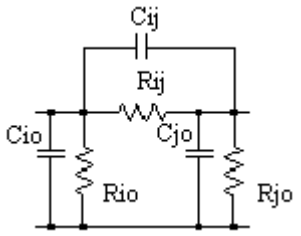

Fig. 1: Simplex element equivalent electrical circuit.

Matrix *N* is associated with the shape of the element (linear, quadratic…), and matrix *B* with the spatial derivative of *N*. *f(t)* and *g(t)* are boundary conditions in edges of low-doped zone, [1].

Using simplex elements, (1), it results:

$$[C(e)]=\frac{A_e L_{Ee}}{6D}\begin{bmatrix}2 & 1\\ 1 & 2\end{bmatrix} (6);\ [G(e)]=\frac{A_e}{L_{Ee}}\begin{bmatrix}1 & -1\\ -1 & 1\end{bmatrix}+\frac{A_e L_{Ee}}{6D\tau}\begin{bmatrix}2 & 1\\ 1 & 2\end{bmatrix} (7);\ [I(e)]=-f(t)A_1-g(t)A_{n+1} \ (8)$$

An electrical circuit implementing these equations is shown in Fig. 1. Applying *KVL* [1]:

$$C_{ij}=C_{ji}=-\frac{A_e L_{Ee}}{6D};C_{io}=C_{jo}=\frac{A_e L_{Ee}}{2D} \ (9);\ R_{io}=R_{jo}=\frac{2D\tau}{A_e L_{Ee}};R_{ij}=R_{ji}=\frac{6D\tau L_{Ee}}{6D\tau A_e-A_e L_{Ee}^2} \ (10)$$

Each net corresponds to *FEM* formulation for one element. Voltages in each node, of this net, are an image of hole/electron concentration. To solve *ADE* it is just needed:

1. A *RC* subcircuit that emulates one element. Number of *RC* nets (subcircuits) in series equals number of elements adopted in partition of the domain (low doped zone).
2. A subcircuit for calculus of element width, L_{Ee}.

Note that:

1. Width of each element, L_{Ee}, is a subcircuit parameter. So they are used smaller elements near the borders, where concentration changes faster, and larger near the middle, where concentration changes slower.
2. Physical/electrical properties, D and τ, in each element, can also be subcircuit parameters which enables solutions for heterogeneous materials.
3. It is easy to add more elements to the problem (just adding another subcircuit).
4. Matrix *I(e)* is nonzero only at the borders (first and last node). So, they are added to these nodes two current sources with values *f(t)A1* and *g(t)An*, satisfying boundary conditions.

2.1 One Finite Element *RC* Net Equivalent *SPICE* Subcircuit

For simulation, in *SPICE* like simulators, they must be designed circuits that emulate variable resistors and capacitors (note that element width, L_{Ee}, varies in time). Circuit topology for one complete *RC* net, for one simplex element, can be seen in Fig. 2. It is made of associating six subcircuits (three variable resistors and three variable capacitors).

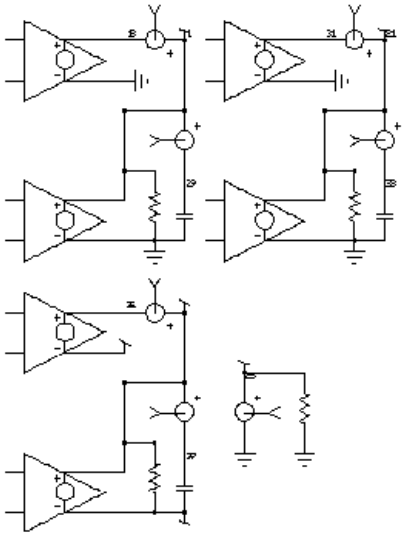

Fig. 2: Equivalent RC net for one finite element.

Subcircuit SPICE code for ICAPS is the following:

```
*SYM=RC\_VAR\_1 1 21 25
DWG=C:\TEXT\ASA\SPICE\CIR\RC_VAR_1.DWG
SUBCKT RC_VAR_1 1 21 25
*ALIAS I(V15)=IVCNT
*This implements Ri0
B3 18 0 V={2*D*TAU}}/({AE}*I(V15))*I(V8)
V8 1 18 DC 0
*This implements Ci0
B4 1 0 I=I(V9)*(I(V15)*1E6-1)
C5 29 0 1E-6*{AE/(2*D)}
V9 1 29 DC 0
R15 1 0 10MEG
*This implements Rj0
B5 31 0 V={2*D*TAU}/({AE}*I(V15))*I(V10)
V10 21 31 DC 0
*This implements Cj0
B6 21 0 I=I(V11)*(I(V15)*1E6-1)
C6 33 0 1E-6{AE/(2*D)}
V11 21 33 DC 0
R16 21 0 10MEG
*This implements Rji
B7 35 21
V=6*{D*TAU*AE}*I(V15)*I(V12)/
({AE}*(6*{D*TAU}/1E4-I(V15)^2))
V1 21 35 DC 0
*This implements Cji
B8 1 21 I=I(V13)*(I(V15)*1E6-1)
C7 37 21 -1E-6{AE/(6*D)}
V2 1 37 DC 0
R17 1 21 10MEG
*This implements LEE
V15 25 0 DC 0
R18 25 0 1K
.ENDS
```

Notice current in zero voltage *DC* source, *V15*, which measures element width, L_{Ee}. During recovery, element width, L_{Ee}, tends to zero, so *0,1U* constant and *10MΩ* resistors to help convergence. Element area, A_e, ambipolar diffusivity, D, and hole/electron mean lifetime, τ, are passed as circuit parameters (see how easy it's to change the properties of the domain for each finite element).

2.2 Element Width Calculus SPICE Subcircuit:

Calculus of instantaneous element width, during recovery, is made with subcircuit shown in Fig. 3. Base width is emulated with a current obtained by a feedback scheme, that imposes zero concentration at the borders [6], [7]. Element width is obtained by resistive division. Note that *I(V10)* is the result of current summing in two high value resistors inserted into space charge boundaries (first and last nodes). This current is measured, passed to *B1*, and multiplied by a high value gain (if node concentration is less than zero).

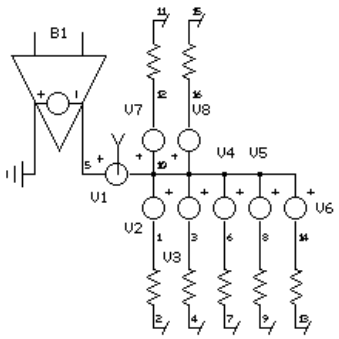

Fig. 3: Subcircuit for calculus of element width.

Subcircuit *SPICE* code (for seven elements) is the following:

```
*SYM=LEE_1 1 21 25
SUBCKT LEE_1 1 21 25
*ALIAS I(V1)=WB-WSC
*Element current division:
R1 1 2 1K
R2 3 4 1K
R3 6 7 1K
R4 8 9 1K
R5 11 12 1K
R6 13 14 1K
R7 15 16 1K
*Space charge zone width calculus, N-=WB-WSC:
B1 0 5 I=I(V10)>0 ? 9M-1.5E4*I(V10) : 9M
V1 5 10 DC 0
*Element width calculus:
V2 10 1 DC 0
V3 10 3 DC 0
 V4 10 6 DC 0
 V5 10 8 DC 0
V6 10 14 DC 0
 V7 10 12 DC 0
V8 10 16 DC 0
.ENDS
```

3 Circuit solvers for remaining zones

In order to implement power semiconductor model they must be designed subcircuits that implement solutions for remaining zones of the devices (dynamics of charge storage effects, highly doped emitters, voltage drops and MOS zones). These are implemented with charge-control principles, recombination sinks (*h* parameters), Boltzmann approach, knowledge of Poisson's equation for time/space carrier concentration and standard *MOS* models [1].

3.1 Narrow Bipolar Transistor *P* Base Zone *SPICE* Circuits

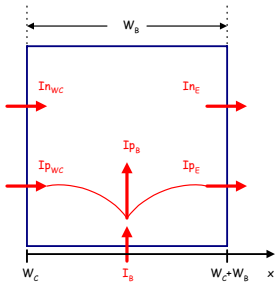

Fig. 4: Currents associated with p base.

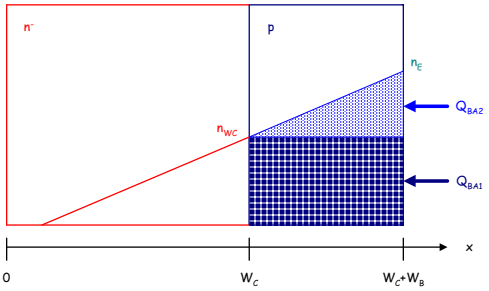

Fig. 5: Base stored charges.

Currents and charges associated with Bipolar Transistor *p* base (see Fig. 4 and Fig. 5) leads to:

$$I_B = I_{pE} - I_{pWC} + I_{pB} \quad (11); \quad I_C = I_{pWC} + I_{nWC} \quad (12),$$

$$I_{pB} = \frac{Q_{BA}}{\tau_B} + \frac{\partial Q_{BA}}{\partial t}; I_{nWC} = qS_E D_{nB} \frac{(pn)_E - (pn)_C}{Q_B + Q_F}$$
$$Q_{BA} = Q_{BA1} + Q_{BA2} = qS_E W_B p_{WC} + \frac{W_B^2 I_{nWC}}{4D_{nB}} \quad (13)$$

So hole base current, I_{pB}, depends on:

1. Hole concentration, p_{wc}, at collector/base boundary.
2. Free electron current, I_{nWC}, at the same boundary.

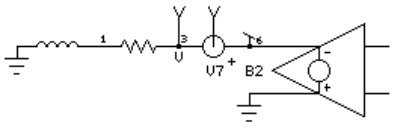

Fig. 6: Circuit for I_{pB} calculus.

Implementation in *SPICE* simulator uses circuits in Fig. 6 and Fig. 7. *Spice* code for calculus of I_{pB} current (Fig. 6) is:

```
*ALIAS V(3)=VX
*ALIAS I(V7)=QBA
*V7 MEASURES QBA*1E6
V7 6 3 DC 0
*INJECTS I=1E6*QBA=K1*PC+K2*INC
B2 0 6 I=475.2M*V(4)+16.875M*I(V6)
*R2 VALUE IS 1E-6/TAU
R2 1 3 .05
*L2 MULTIPLIES BY1E-6
L2 1 0 1E-6
```

Notice that *V(4)* measures p_{wc} and *I(V(6))* measures I_{nWC}. Both are available in circuit of Fig. 7.

Spice code for calculus of I_{nWC} current (Fig. 7) is:

```
*ALIAS I(V2)=IPC
*ALIAS I(V3)=IPB
*ALIAS I(V4)=IPE
*ALIAS I(V6)=INC
*V2 MEASURES IPC=IPB+IPE-IB
```

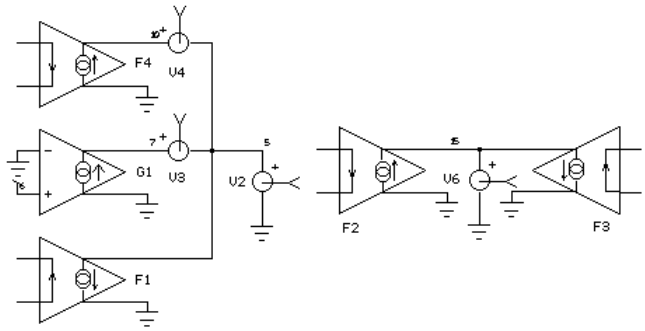

Fig. 7: Circuit for I_{nWC} calculus.

```
V2 5 0 DC 0
*V3 MEASURES IPB
V3 7 5 DC 0
*V4 MEASURES IPE
V4 10 5 DC 0
*V6 MEASURES INC
V6 15 0 DC 0
*G1 CONVERTS VX IN CURRENT IPB (IPB=VX)
G1 0 7 6 0 1
*F1 INJECTS IB (MEASURED IN V56)
F1 5 0 V56 1
*F2 INJECTS IC (MEASURED IN V5)
F2 0 15 V5 1
*F3 INJECTS IPC (MEASURED IN V2)
F3 15 0 V2 1
*F4 INJECTS IPE (MEASURED IN V64)
F4 0 10 V64 .44
```

Notice that I_C is injected by *F2*, I_B by *F1* and I_{pE} by *F4*. These are available in other zones of the circuit.

3.2 III.B-Highly Doped N+ Emitter Circuit

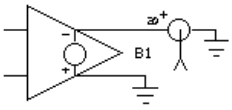

Fig. 9: Circuit for I_{pE} calculus.

```
*ALIAS I(V64))=PNE
V64 20 0 DC 0
*PNE=PC^2+I
NC*(QBD+QBA)/((Q*SE)^2*DNB)
B1 0 20 I=V(4)*V(4)+.2988*I(V6)*(0.165+I(V7))
```

Notice that *V(4)* measures p_{wc}, *I(V(6))* I_{nwc} and *I(V(7))* Q_{BA}.

h parameter approximation gives:

$$I_{pE} = qS_E h(pn|_E) = qS_E hp_{wc}^2 + \frac{hI_{nwc}[Q_{BD} + Q_{BA}]}{qS_E D_{nB}} \qquad (16)$$

Therefore, hole current in emitter depends on:

1. Hole concentration, p_{wc}^2, at collector/base boundary.
2. Electron current, I_{nwc}, at the same boundary.
3. Base charges, Q_{BD}, Q_{BA}, solved with charge control methods.

Fig. 9 shows the circuit. and associated code implementation as a nonlinear controlled source.

3.3 Voltage Drops

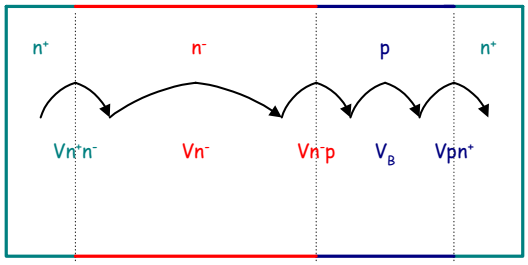

Fig. 10: *npn BJT* voltage drops

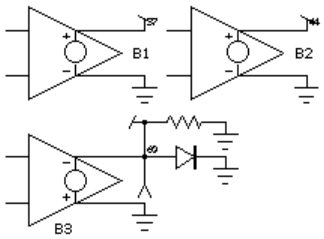

Fig. 11: Circuit for V_{pn+}, V_{n+n-} and V_{n-p}. calculus.

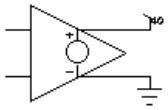

Fig. 12: Circuit for calculus of voltage drop in one *RC* net element.

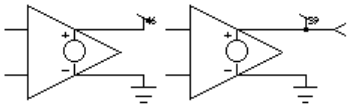

Fig. 13-Circuit for calculus of V_{SC} .

Boltzmann approach, knowledge of time/space carrier concentration and Poisson equation gives the following expressions for voltage drops calculus (see Fig. 10), [1]:

$$V_{pn+} = V_T \ln\left(\frac{p_E n_E}{n_i^2}\right) (17) \quad V_{n+n-} = V_T \ln\left(\frac{p_0}{N_C}\right) (18) \quad V_{n-p} = 2V_T \ln\left(\frac{p_{WC}}{n_i^2}\right) (19) \quad V_{n-} = \int_{Xl}^{Xr} \frac{J_n}{q\mu_n n} \partial x \ (20)$$

$$V_{SC} = \frac{qN_C}{2\varepsilon} W_C^2 \ (21)$$

So it must be got $p_E n_E$ (given by *I(V(64)*, see 1.1), p_0 and p_{WC} (given in first and last nodes of our *RC* net *V(2)* and *V(4)*, see 2.1), J_n and width of space charge zone W_C (given in *V1*, see 2.2).

SPICE implementation takes the form of nonlinear controlled sources (see Fig. 11 and Fig. 12).

Spice code for calculus of V_{n+n-} V_{n-p} and V_{pn+}, is:

```
*DIODE MODEL
.MODEL DPNE D(IS=1.44E-14)
*ALIAS V(60)=VBEI
*IMPLEMENTS VN+N-=VT*LOG(P0/NC);
 C=1.2E15
B2 44 0 V=V(4)>0 ? 26E-
3*LN((V(4)*1E2+1.2)/1.2) : 0
*IMPLEMENTS VN-
P=2*VT*LOG(PWC/NI^2);
I=1.2E10
B1 37 0 V=V(2) >0 ? 52E-
3*LN((V(2)*1E7+1.44)/1.44) : 0
*IMPLEMENTS
VPN+=VT*LOG(PE*NE/NI^2)
PE*NE=I(V64)
D1 60 0 DPNE
B3 0 60 I=I(V64)
R1 60 0 470
```

Spice code, for calculus of ohmic voltage drop along one *n-* collector element is (this is similar for all elements):

```
*ALIAS V(80)=RTOTAL
.PRINT DC V(80)
.PRINT TRAN V(80)
B3 40 0 V=V(4)>0 ?
I(V8)/((V(4)+V(15))*1E3*1347+VNC1) : VNC1
*LE1/(2*PAV1*NIUNP+2*NIUN*ND
```

Spice code for calculus of V_{SC} is:

```
*ALIAS V(39)=VSC
*VSC2=K4*(WC-XSC)^2
B2 39 0 V=I(V4)>0 ? 5.84E6*I(V58)^2: 0
*VSC1=58604*I(V58)*LN(1+EXP(7.54-
3077*(8.2M-I(V58))))
B1 46 0V=I(V4)>0?
58604*I(V58)*LN(1+EXP(7.54-3077*(8.2M-
I(V58)))) : 0
```

3.4 *MOSFET* model

3.4.1 *MOS* current

MOS part of devices is well represented with standard *MOS* models. For *DC* characteristics, a basic expression for channel current is:

in linear region:

$$I_{mos} = K_p\left[\left(V_{gs} - V_{th}\right)V_{ds} - \frac{V_{ds}^2}{2}\right] \quad (22)$$

in saturation region:

$$I_{mos} = \frac{K_p\left(V_{gs} - V_{th}\right)^2}{2} \quad (23)$$

This model can be improved taking in account several important phenomena such as:

1. Transconductance reduction in linear region.
2. Mobility reduction due to transverse electric field for high gate voltages.
3. Avalanche breakdown for high drain voltages.

These effects are modeled introducing, respectively:

1. $K_{p_{lin}}$, empirical parameter .
2. θ, empirical parameter that represents the reduction of transconductance.
3. M, avalanche multiplication factor.

Thus, the above equations are rewritten as:

$$I_{mos} = K_{p_{lin}}\left[\left(V_{gs} - V_{th}\right)V_{ds} - \frac{K_{p_{lin}}V_{ds}^2}{2K_{p_{sat}}}\right]\times\frac{M}{1+\theta\left(V_{gs} - V_{th}\right)} \qquad V_{ds} < \left(V_{gs} - V_{th}\right)\frac{K_{p_{sat}}}{K_{p_{lin}}} \qquad M = \left[1 - \left(\frac{V_{ds}}{V_{br}}\right)^4\right]^{-1}$$

$$I_{mos} = \frac{K_{p_{sat}}\left(V_{gs} - V_{th}\right)^2}{2}\times\frac{M}{1+\theta\left(V_{gs} - V_{th}\right)} \qquad V_{ds} > \left(V_{gs} - V_{th}\right)\frac{K_{p_{sat}}}{K_{p_{lin}}} \qquad V_{br} = 5{,}34\times10^{13}\,k_v N_D^{-0{,}75}$$

3.4.2 MOS capacitances

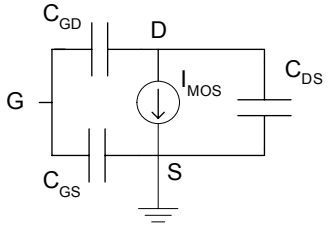

Fig. 14: MOSFET part of IGBT

Transient behavior is ruled by capacitances between device terminals as illustrated in Fig. 14

Well-known nonlinear Miller capacitance is the most important one in order to describe swhiching behavior of MOS part. It is comprehended of a series combination of gate-drain oxide capacitance (C_{ox}) and gate-drain depletion capacitance (C_{gdj}) resulting in equation (22).

$$C_{gd} = \frac{C_{ox}}{1 + \frac{W_{sc}^{'}C_{ox}}{\varepsilon_{si}A_{gd}}} \text{ with: } W_{sc}^{'} = \sqrt{\frac{2\varepsilon_{si}V_{gd}}{qN_D}}\,. \quad (24).$$

Being W'_{sc} depletion width formed under the gate, N_D base doping concentration and A_{gd} is MOS region area. Drain-source capacitance (C_{ds}) is defined in the same way as C_{gdj} , being W_{sc} total depletion width developed under p^+ body and A_{ds} the respective area (see (23). Note that A_{gd} + A_{ds} represents total device area (A). As depletion zone widths support different voltages and remembering that $V_{gd} = V_{ds} - V_{gs}$ relations (24) can be written.

$$C_{ds} = \frac{\varepsilon_{si}A_{ds}}{W_{sc}} \text{ with: } W_{sc} = \sqrt{\frac{2\varepsilon_{si}V_{ds}}{qN_D}}\,. \quad (25)$$

$$\begin{cases} W_{sc}^{'} = 0 & W_{sc} < \sqrt{\frac{2\varepsilon_{si}V_{gs}}{qN_D}} \\ W_{sc}^{'} = \sqrt{W_{sc}^2 - \frac{2\varepsilon_{si}V_{gs}}{qN_D}} & W_{sc} > \sqrt{\frac{2\varepsilon_{si}V_{gs}}{qN_D}} \end{cases}. \quad (26)$$

Gate-source capacitance is normally extracted from capacitance curves and a constant value may be used producing generally good results [10].

4 Implementation in SPICE

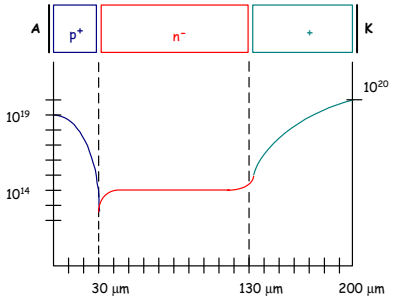

Fig. 15: Typical power diode doping profile and width of the *p*, *n* zones.

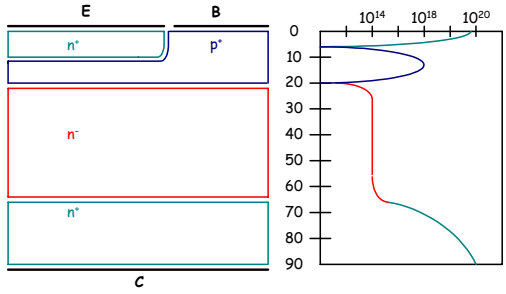

Fig. 16: Typical power BJT doping profile and width of the *p*, *n* zones.

They can now be applied given fundamentals for modeling bipolar power semiconductors. Fig. 15 and Fig. 16 shows, as an example, power diode and *BJT* zones to model.

4.1 POWER *P-I-N* DIODE *SPICE* MODEL

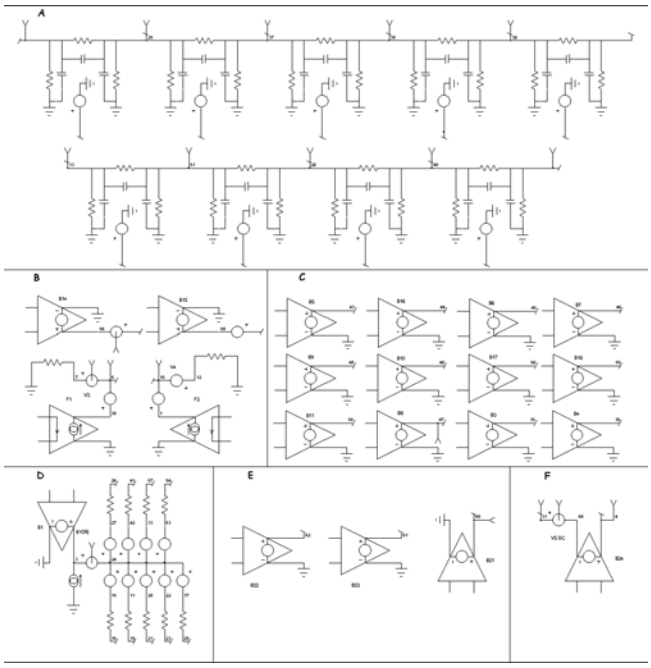

Fig. 17: Diode model.

A complete nine finite element power p-I-n diode model (9 *RC* nets) for power *p-I-n* diode simulation can be seen in Fig. 17. This model uses in *A* the circuit solution for low doped zone, in *B* circuit solution for current at *n*- zone borders (emitter currents in *n*+ and *p*+ zones with *h* parameter approach), in *C* circuit for voltage drops calculation. Part *D* solves for base (*n*- zone) and element width and *E* for voltage drops in space charge zones. Finally *F* is diode connection to external circuit with voltage controlled source V_D.

Note how easy you can change:

1. Number of model elements (one more *RC* net in *A*, one more resistor in *D*, one more source in *C*).
2. Width of elements (just change resistor values in *D*).
3. Properties of *n*- zone (just change parameters A_E, τ, *D* in each *RC* net of *A*).

4.2 POWER *BJT SPICE* MODEL

Fig. 18 shows a complete model for power *BJT* simulation. This nine finite element power *BJT* model uses in *A* the circuit solution for collector low-doped zone, in *B* circuit solution for collector (n- zone) and element width. *C* solves for currents at collector borders (emitter currents in *n*+ and *p*+ zones with *h* parameter approach). *D* and *E* solves for base currents I_{pB}, I_{pWC} and I_{pE}. Finally *F* and *G* solves, for voltage drops. *H* is *BJT* connection to external circuit with controlled voltage sources, V_{CE} and V_{BE}.

Note how easy it can be changed:

1. Number of model elements (one more *RC* net in *A*, one more resistor in *B*, one more source in *G*).
2. Width of elements (just change resistor values in *B*)
3. Properties of n- zone (just change parameters A_E, τ, *D* in each *RC* net of *A*).

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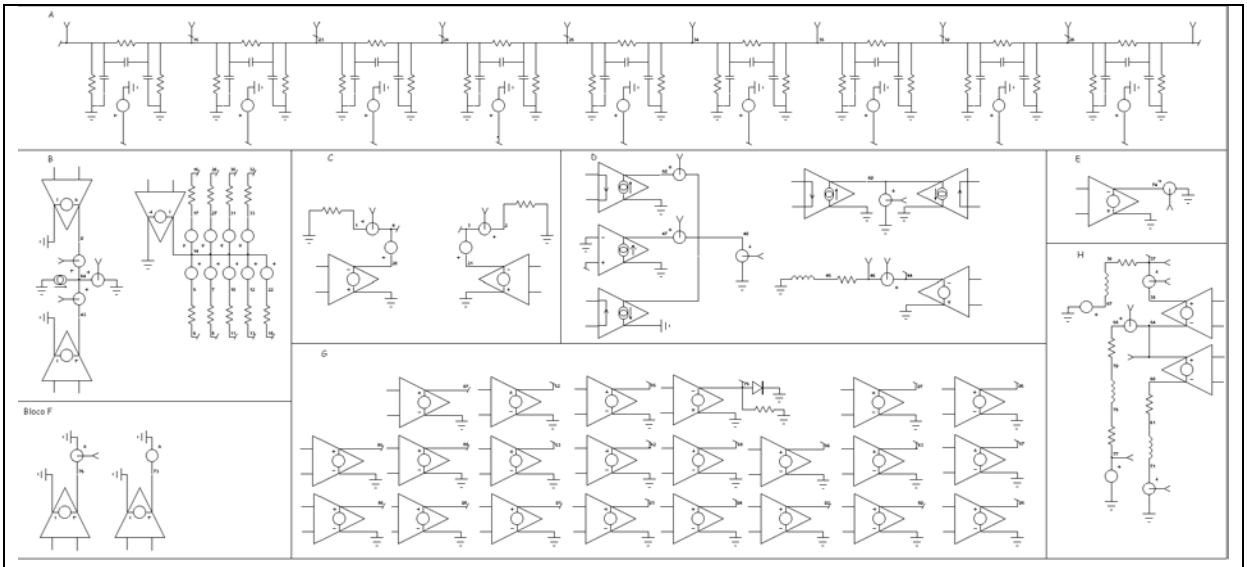


Fig. 18: BJT model

4.3 POWER *IGBT SPICE* MODEL

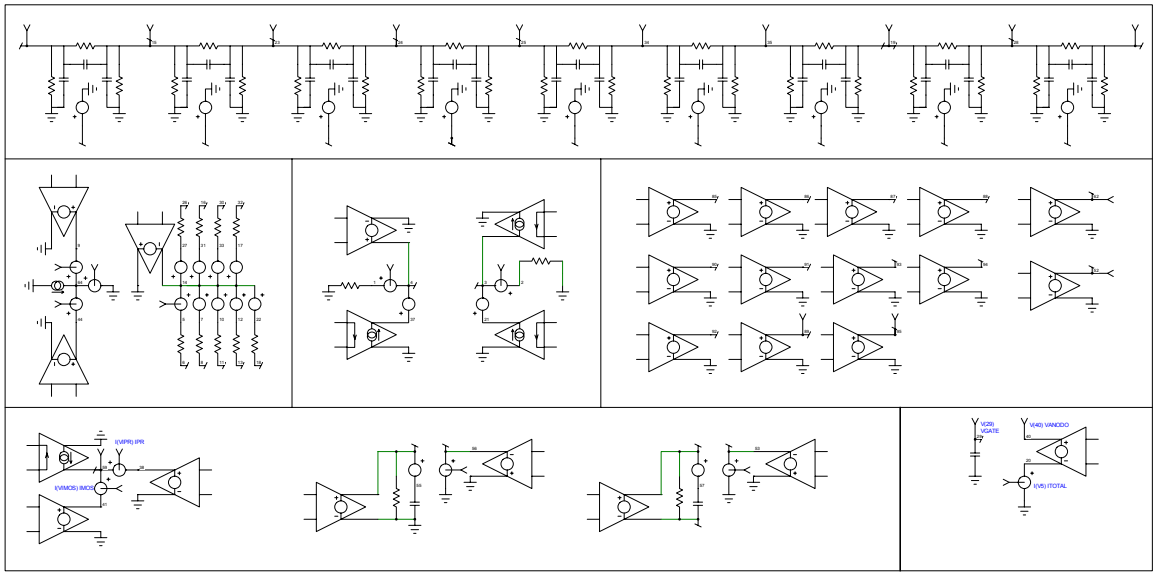


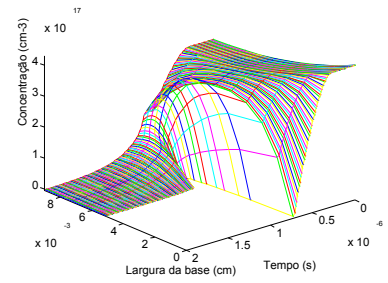
Fig. 19: SPICE FEM based IGBT model.

Fig. 19 shows a complete nine finite element *IGBT* model. Notice, at the top, FEM solution for time/space hole/electron distribution in low-doped *IGBT* base. Controlling parameter l_e is determined by the circuit at middle left and boundary conditions, at borders of *IGBT* base, with circuit in center. Circuit at right middle emulates voltage drops in junctions, space charge and ohmic zones along *IGBT* base. Circuits at left bottom emulate *MOSFET* part of *IGBT*. Circuit at right bottom calculates total voltage drop, so the IGBT is seen as current controlled voltage source.

5 RESULTS

Some results, obtained with these models, are presented in Fig. 20, Fig. 21, Fig. 22, Fig. 23, Fig. 24 and Fig. 25. As a first example Fig. 20 shows reverse recovery simulation results (hole/electron concentration in time and space and current and voltage in time) for a diode with $Nb=1014\ cm^{-3}$, $W_B=90\mu m$, $\tau=10\mu s$, $Dn=25cm^2/s$, $Dp=10cm^2/s$, $h_p=h_n=1.5*10E\text{-}14cm^4/s$. Simulation time is 20 seconds in a 133 MHz PC. Notice evolution of stored charge during first 800 nanoseconds

and concentration fall and space charge evolution after that. Notice also that the solution is for time and space with a circuit simulator!



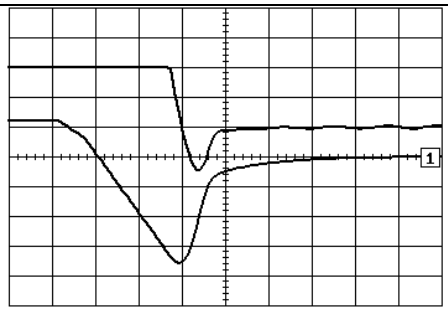
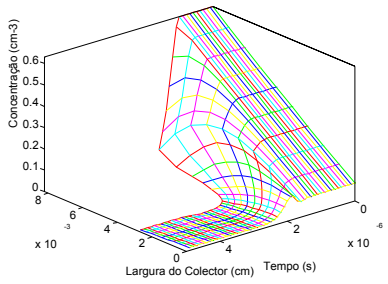


Fig. 20: Diode concentration and reverse recovery current and voltage (10A, 100V, 200ns/div).



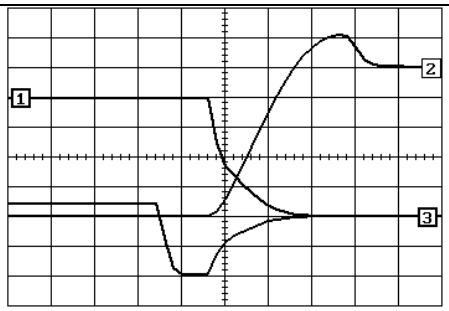


Fig. 21: BJT concentration, VCE voltage, IC and IB currents, at turn-off (50V, 0.5A, 1A, 500ns/div.)

As a second example Fig. 21 presents some results for Motorola power *BJT MJE 18004* during turn-off. Notice that transistor is fully saturated prior to turn-off. Notice also no charge evolution during storage time (from 1750 to 2230 nanoseconds) and concentration fall and space charge evolution after that.

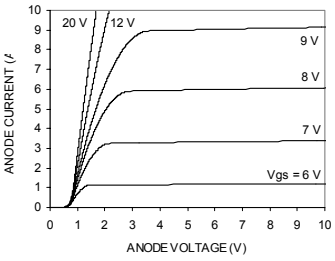


Fig. 22: Simulated static IGBT characteristics.

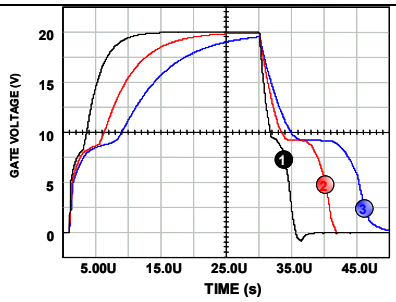


Fig. 23: IGBT gate voltage.

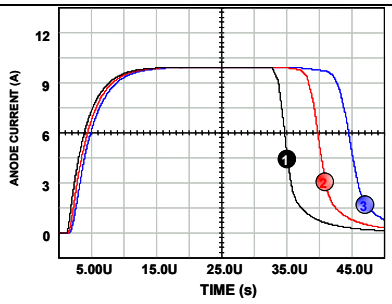


Fig. 24: IGBT anode current.

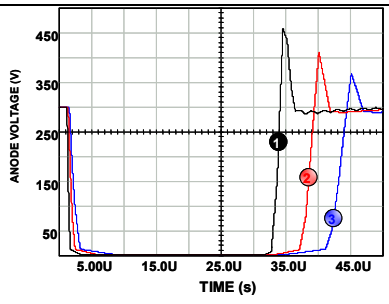


Fig. 25: IGBT anode voltage.

Finally

Fig. 22 to Fig. 25 shows static characteristics simulation and gate voltage, anode current and anode voltage simulation for an IGBT in a test circuit composed with a resistor-inductor load and a resistive gate drive. The test is conducted with V_{cc} = 300V, load inductor of 80 μH, load resistance of 30 Ω and various gate resistances (1, 2 and 3 KΩ).

Notice that IGBT model implements with accuracy:

1. Diode voltage offset due to anode-epitaxial layer p-n junction.
2. Low resistance in on-state (due to conductivity modulation).
3. MOSFET channel current saturation.

Notice that model also predicts all dynamic IGBT characteristics, namely:

1. Slowly decaying current at turn-off (tailing phenomenon characteristic of IGBTs due to bipolar transistor part).
2. Control of node voltage rise through gate resistance.
3. Gate controlled turn-off delay time.

Simulation time, for a complete turn-on/turn-off cycle, is about 2 seconds in a AMD Athlom XP 1800 processor running at 1.5 GHz with 512Kb of RAM.

6 Conclusions

This paper discussed the design of circuits for implementing bipolar power device models. These models solve for *ADE* in time and space, with any *SPICE* like circuit simulator, so dynamics of the devices are well represented. Refinement of model characteristics, such as, non-equally spaced elements, non-homogeneous doping and diffusivities and number and type of elements is a simple task and left as a choice for the user.

Future work on this subject will be development of *FEM* bidimensional model for narrow bases (so it can be adopted a distributed approach instead of charge control models) and, finally, the most ambitious one, coupling the model to the heat diffusion equation also solved with *FEM* and variational approaches in order to have electrothermal models.

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